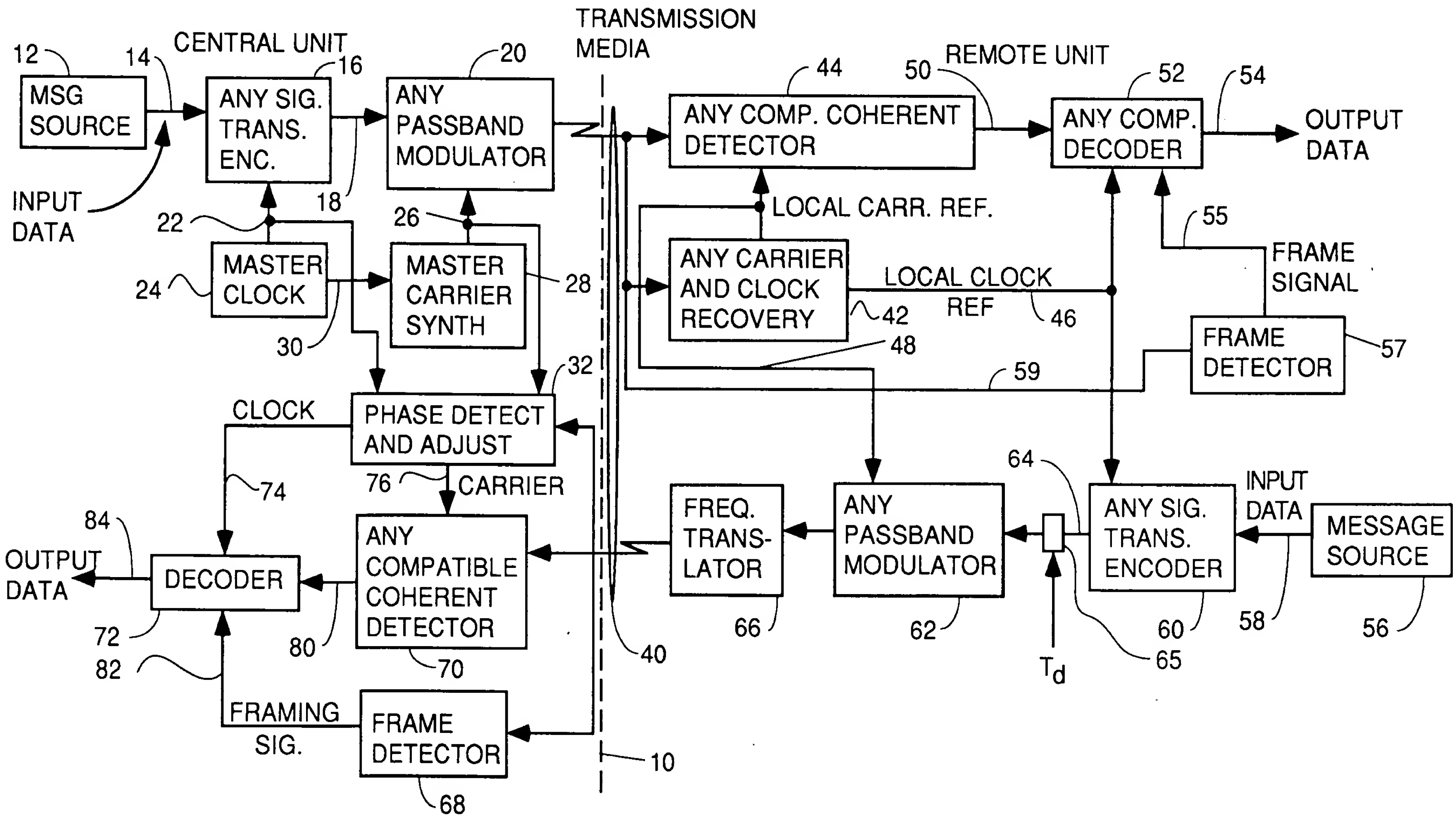
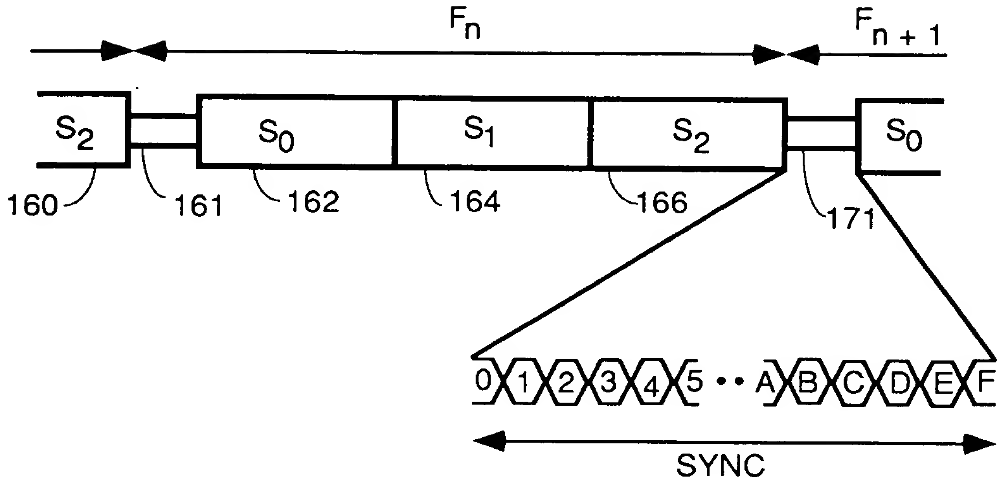


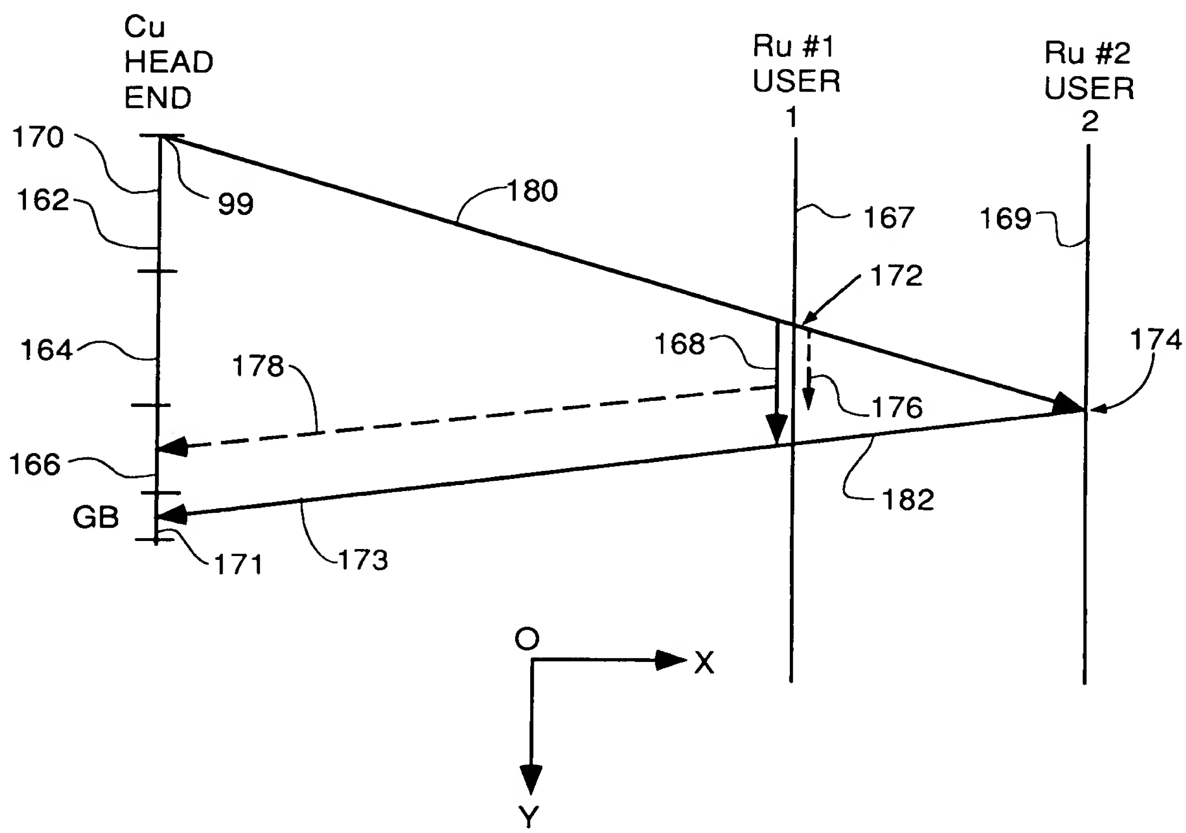
CENTRAL UNIT
TRANSMISSION MEDIA
REMOTE UNIT
MSG SOURCE
INPUT DATA
ANY SIG. TRANS. ENC.
ANY PASSBAND MODULATOR
MASTER CLOCK
MASTER CARRIER SYNTH
PHASE DETECT AND ADJUST
CLOCK
CARRIER
ANY COMPATIBLE COHERENT DETECTOR
DECODER
OUTPUT DATA
FRAMING SIG.
FRAME DETECTOR
ANY COMP. COHERENT DETECTOR
LOCAL CARR. REF.
ANY CARRIER AND CLOCK RECOVERY
LOCAL CLOCK REF
ANY COMP. DECODER
OUTPUT DATA
FRAME SIGNAL
FRAME DETECTOR
FREQ. TRANS-LATOR
ANY PASSBAND MODULATOR
ANY SIG. TRANS. ENCODER
INPUT DATA
MESSAGE SOURCE
T_d
12
14
16
18
20
22
24
26
28
30
32
40
42
44
46
48
50
52
54
55
56
57
58
59
60
62
64
65
66
68
70
72
74
76
80
82
84
10

FIG. 1



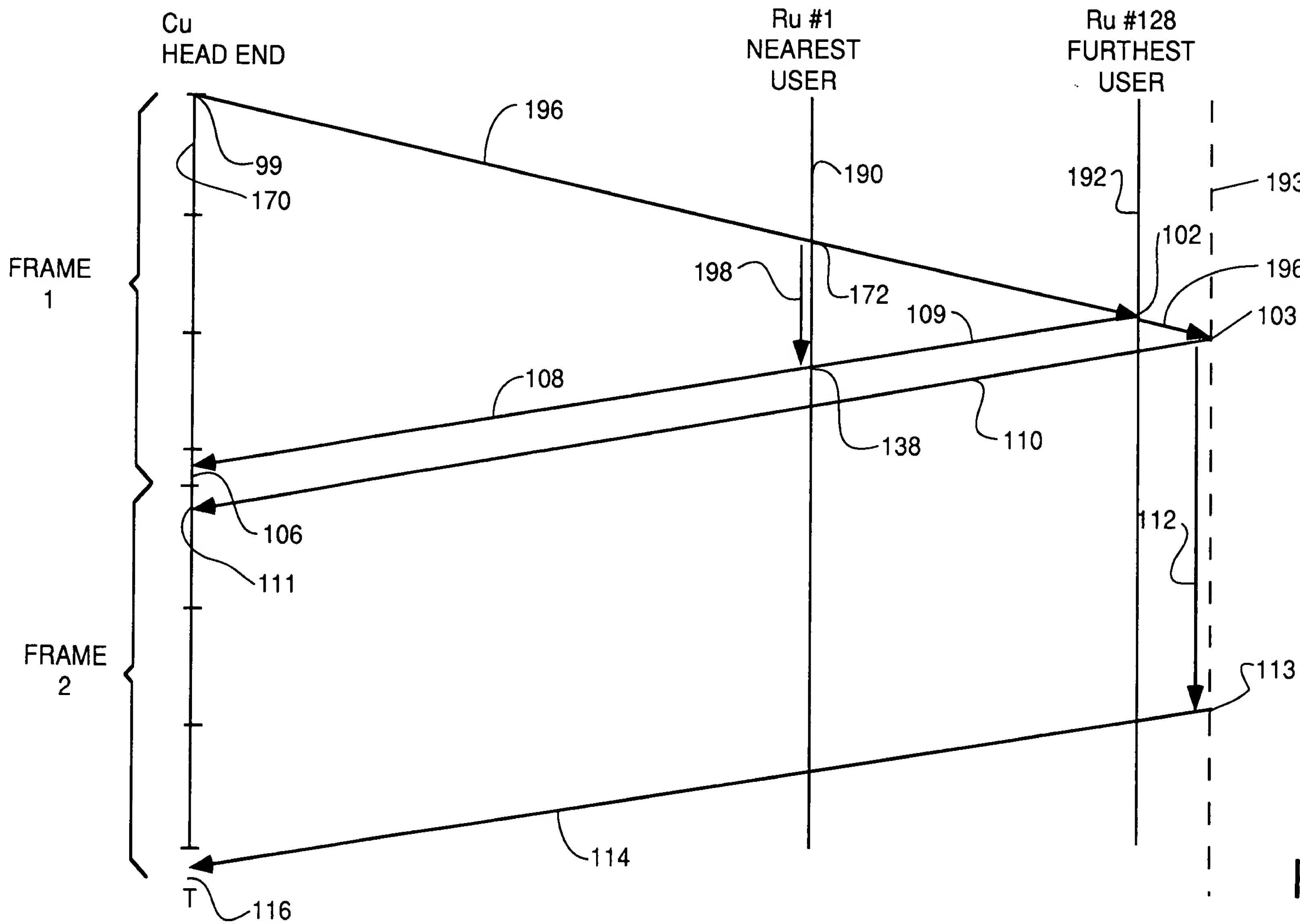
F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 • • A B C D E F
SYNC

FIG. 2A



Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
99
180
167
169
172
164
168
174
178
176
166
182
GB
171
173
O
X
Y

FIG. 2B



Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
196
99
170
190
192
193
102
196
198
172
109
103
108
138
110
106
111
112
113
114
T
116

FIG. 3

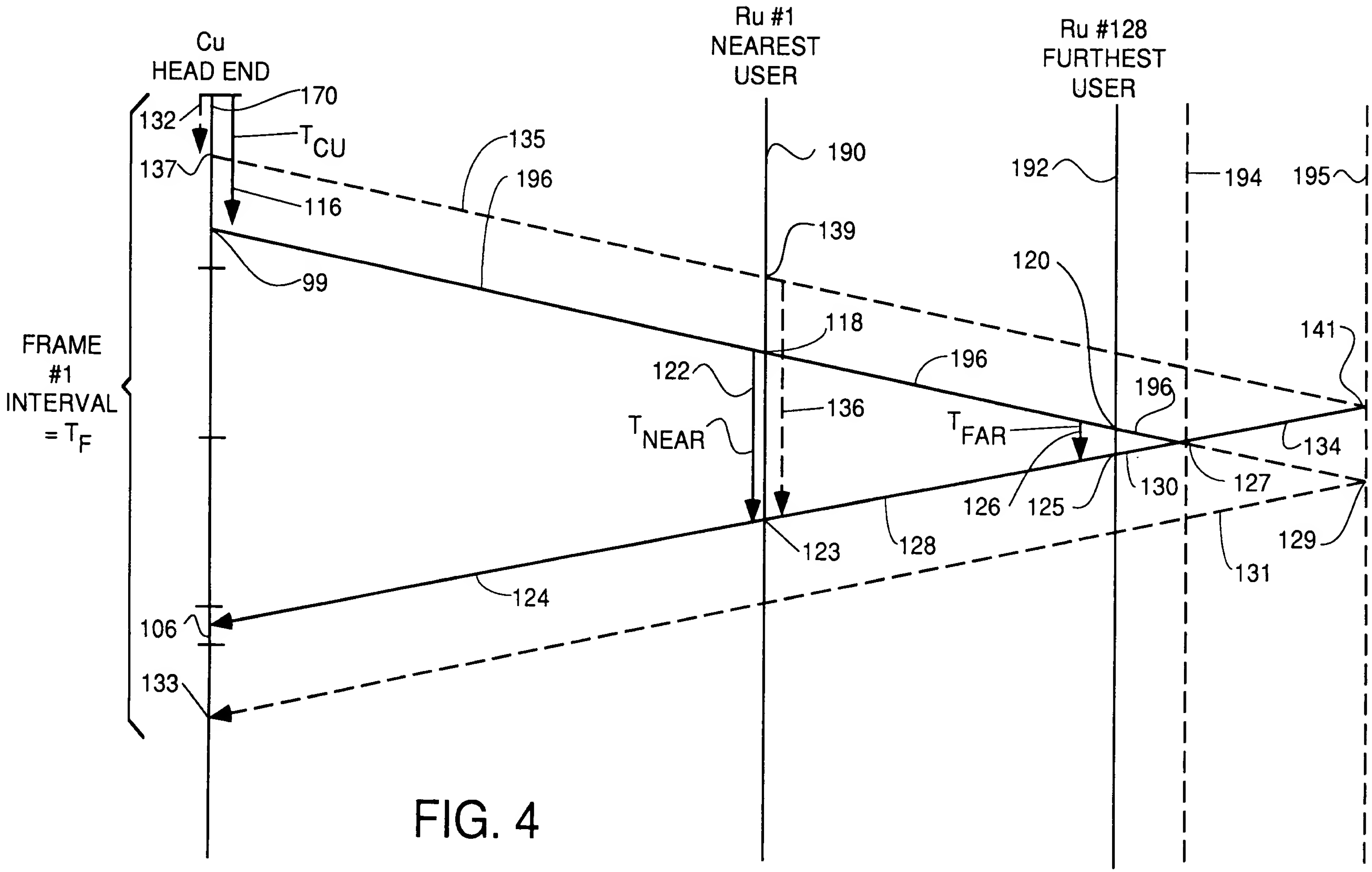
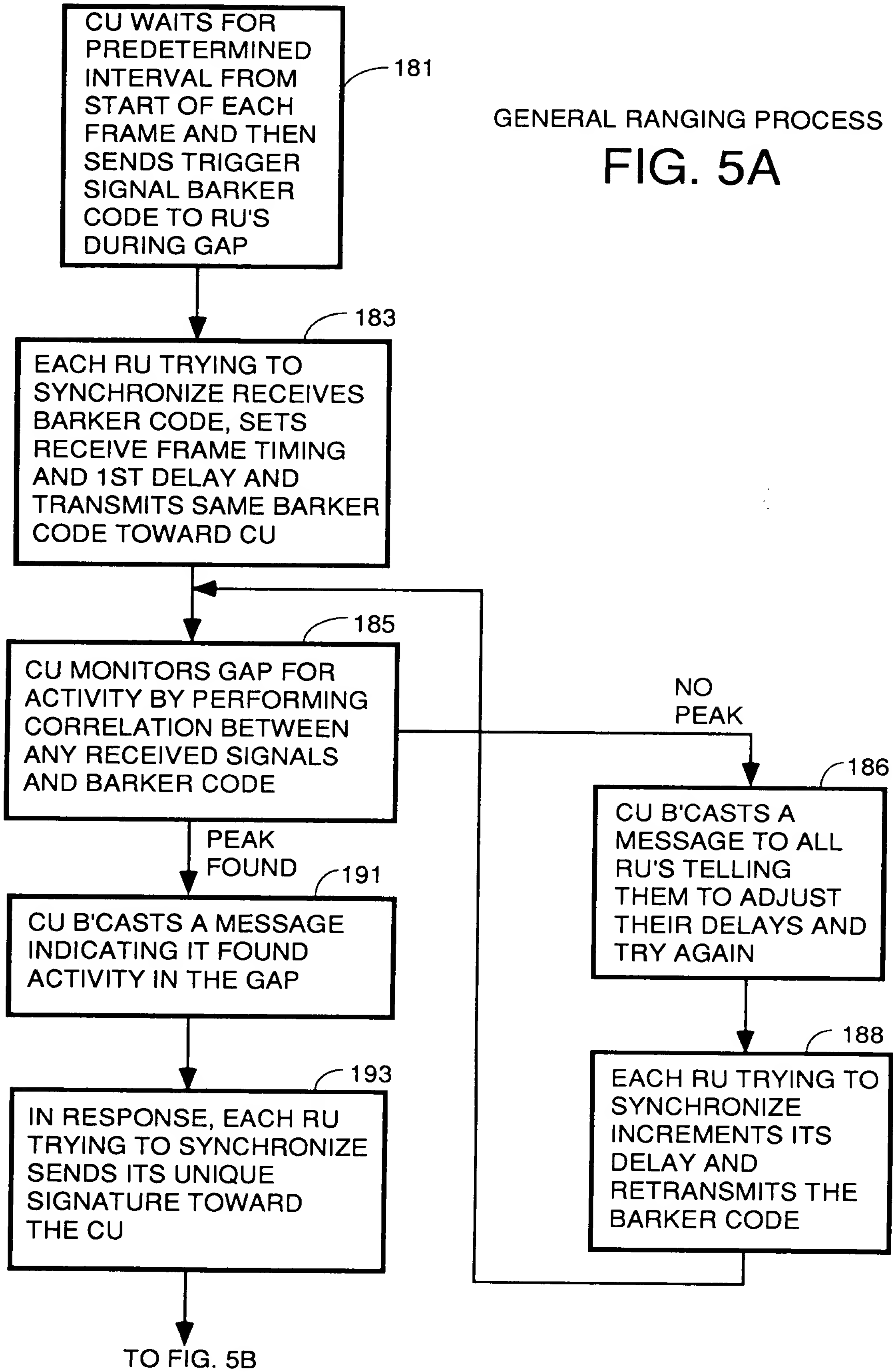

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
#1
INTERVAL
$= T_F$
T_{CU}
T_{NEAR}
T_{FAR}
132
137
170
116
99
135
196
190
139
118
122
136
123
124
106
133
192
194
195
120
141
196
134
127
130
125
126
128
129
131

FIG. 4



GENERAL RANGING PROCESS

FIG. 5A

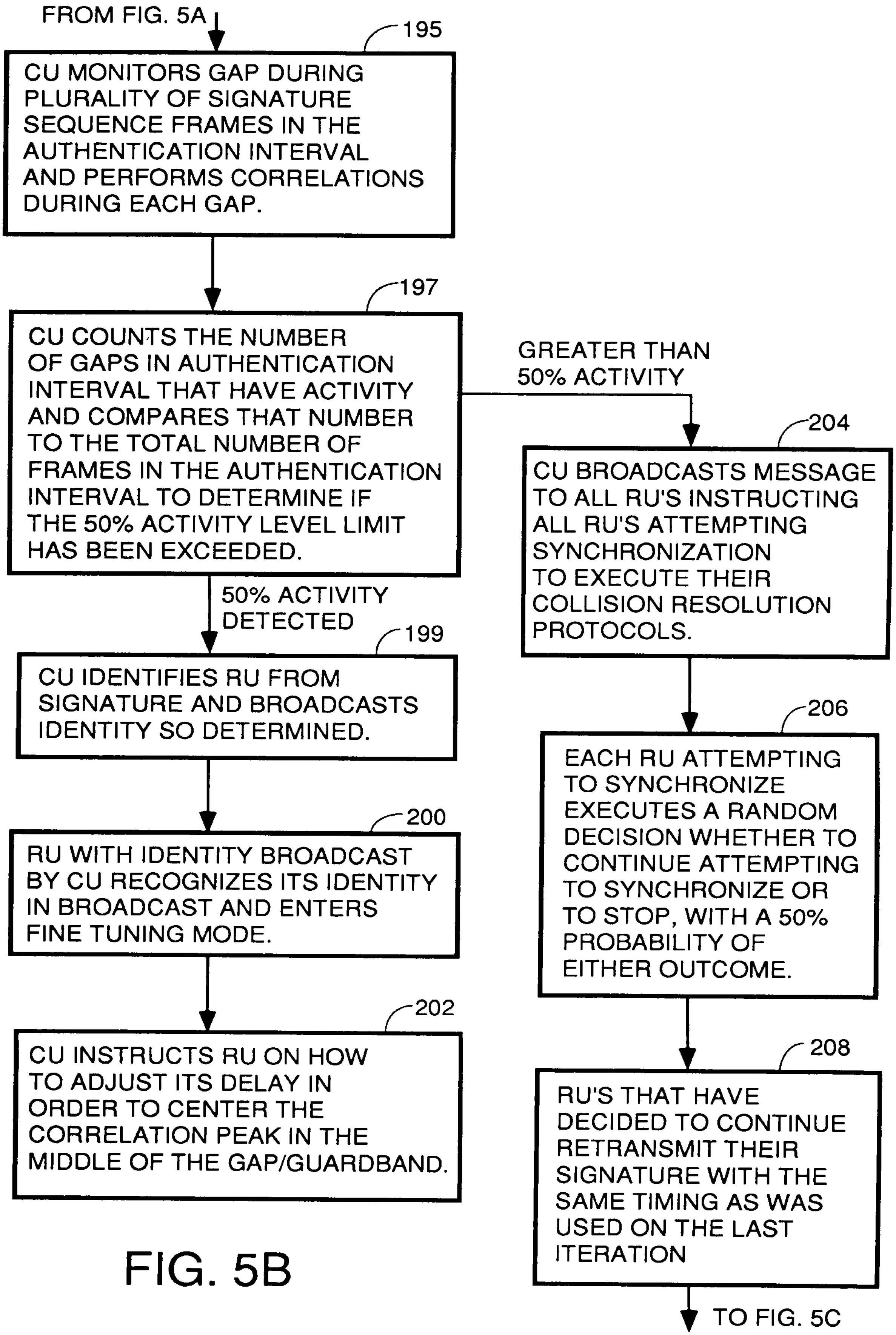

FROM FIG. 5A
195
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
50% ACTIVITY DETECTED
199
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 5C

FIG. 5B

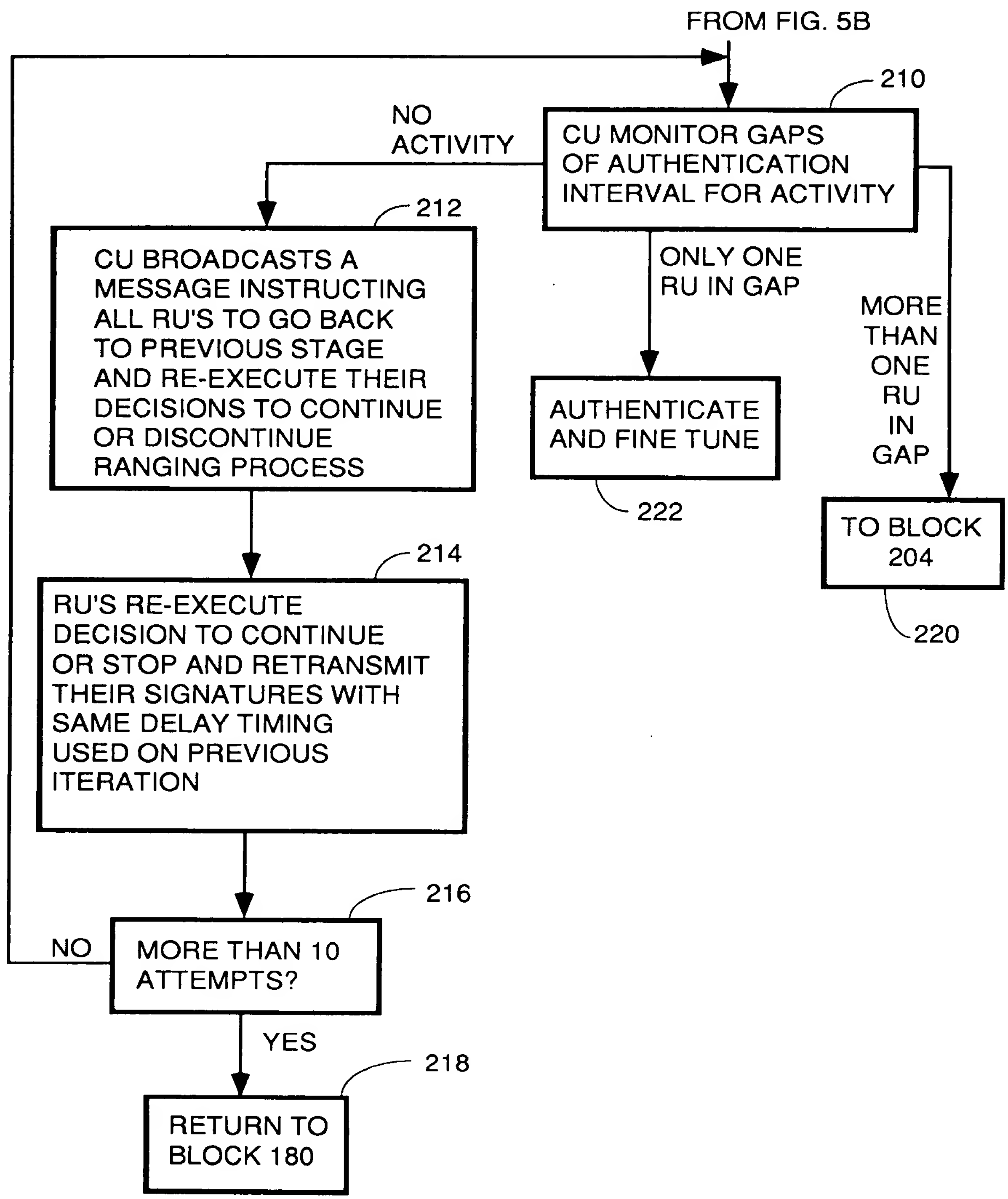

FROM FIG. 5B
210
NO ACTIVITY
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
MORE THAN ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C

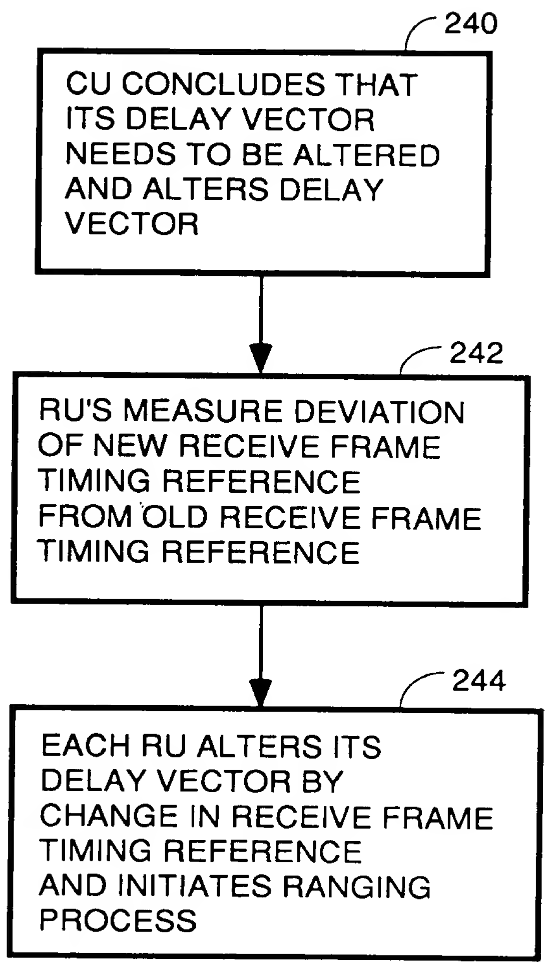


FIG. 6
DEAD RECKONING RE-SYNC

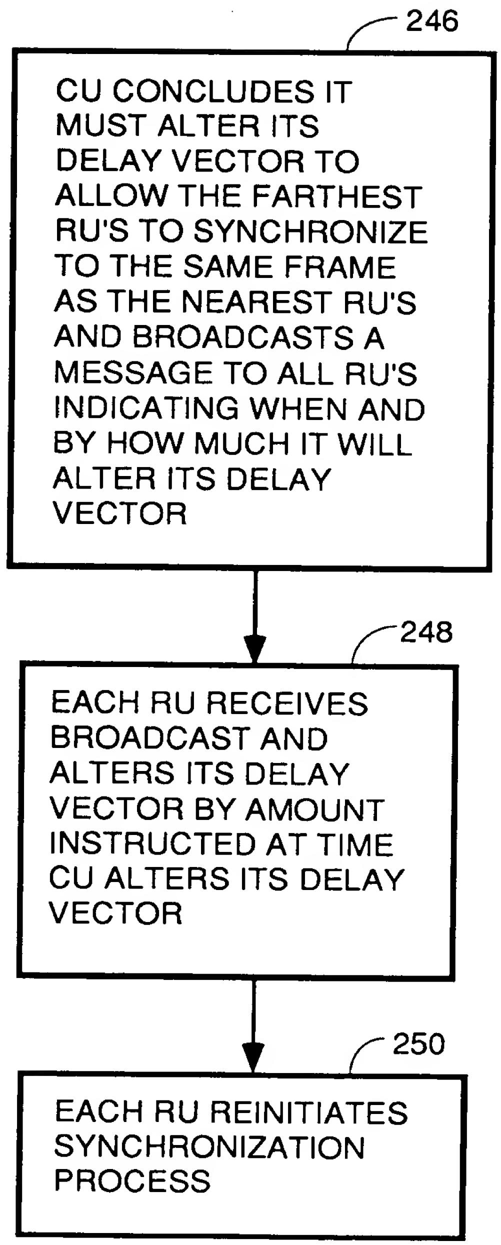
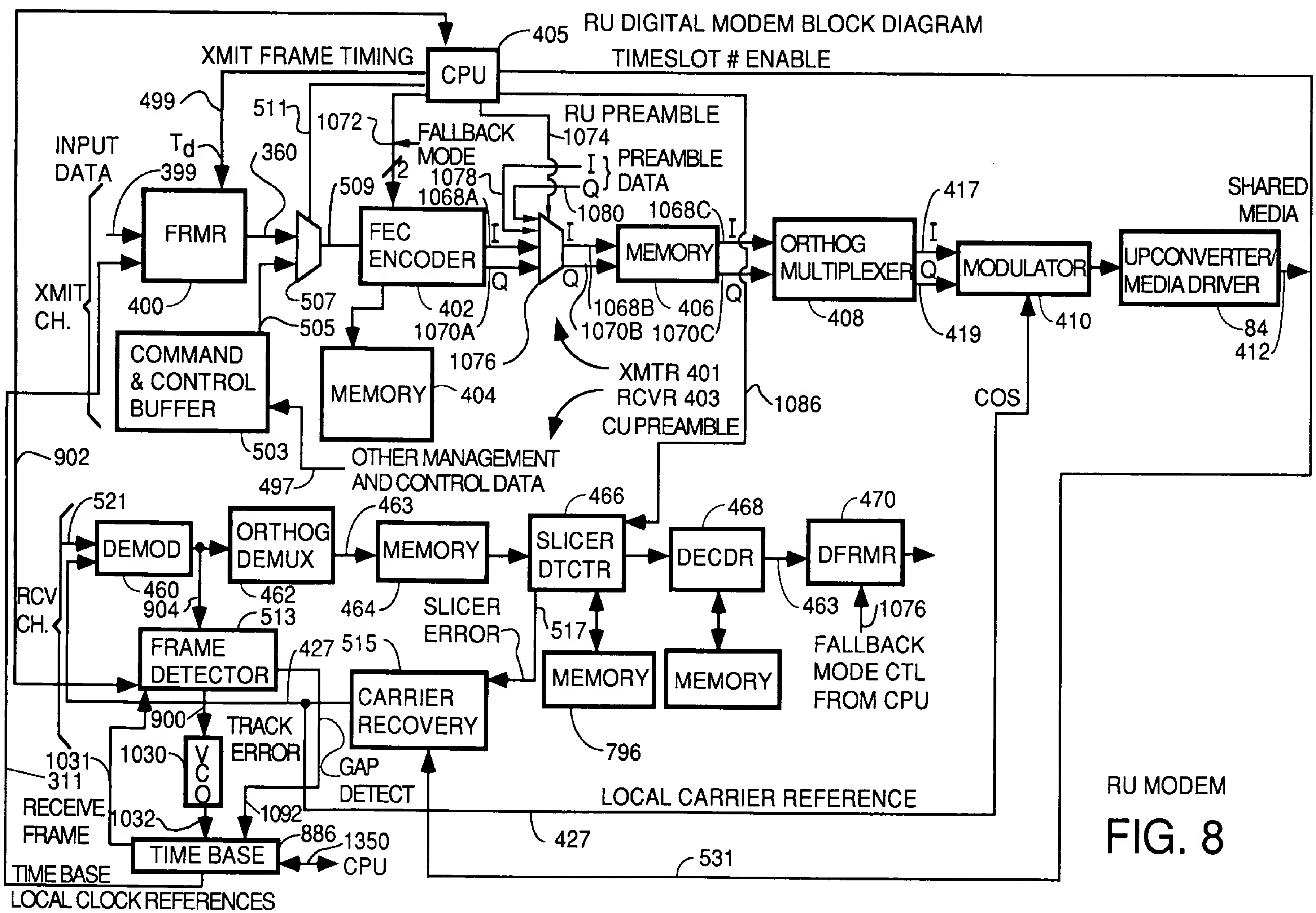
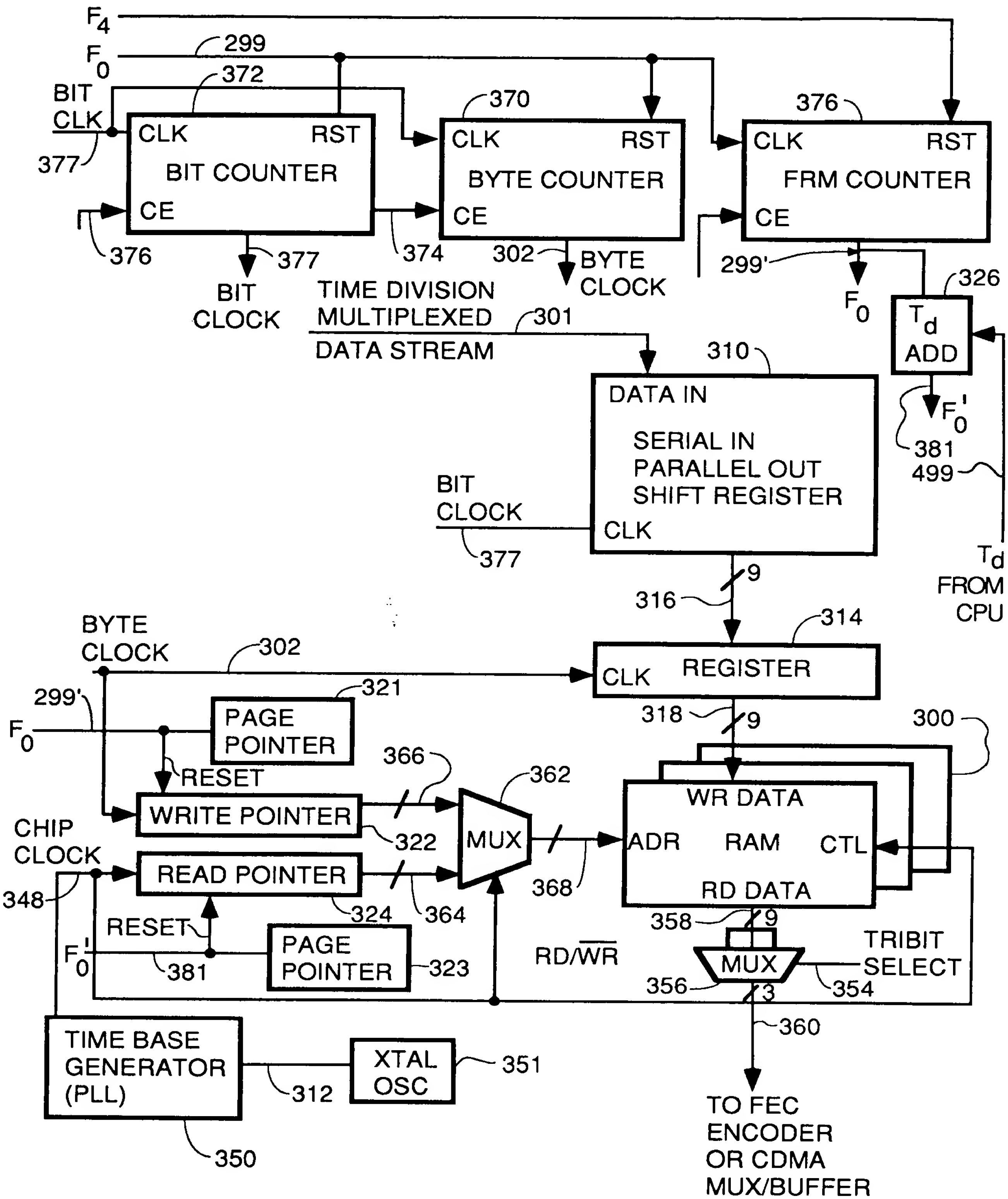


FIG. 7
PRECURSOR EMBODIMENT



RU MODEM

FIG. 8



F4
F0
299
372
BIT CLK
377
CLK
RST
BIT COUNTER
CE
376
377
BIT CLOCK
374
370
CLK
RST
BYTE COUNTER
CE
302
BYTE CLOCK
376
CLK
RST
FRM COUNTER
CE
299'
F0
326
Td ADD
F0'
381
499
Td FROM CPU
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
BIT CLOCK
377
9
316
314
CLK
REGISTER
318
9
300
BYTE CLOCK
302
299'
F0
321
PAGE POINTER
RESET
366
362
WRITE POINTER
322
MUX
CHIP CLOCK
348
READ POINTER
324
364
368
WR DATA
ADR
RAM
CTL
RD DATA
RESET
F0'
381
PAGE POINTER
323
RD/WR
358
9
MUX
TRIBIT SELECT
356
3
354
360
TIME BASE GENERATOR (PLL)
XTAL OSC
351
312
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 9

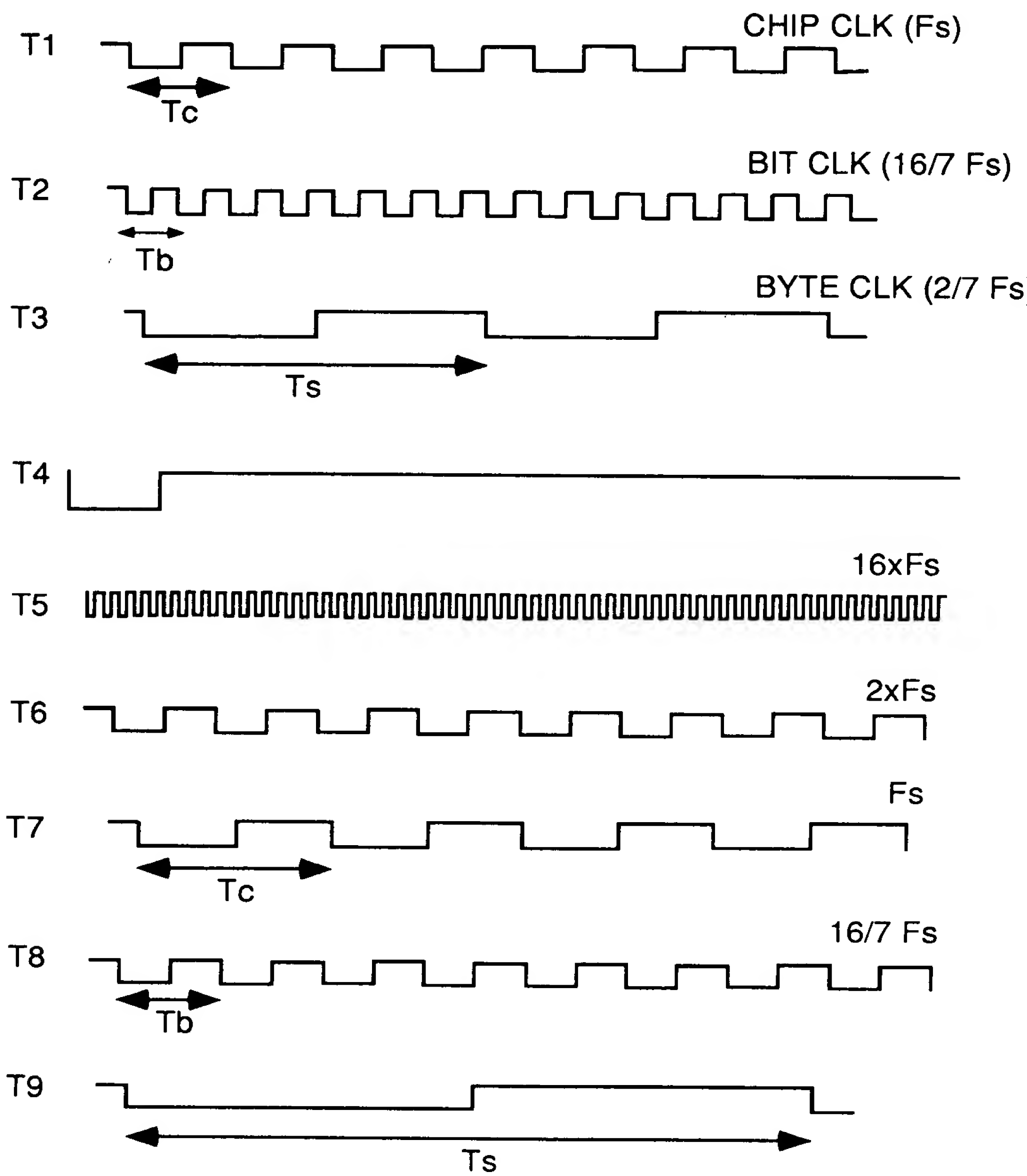

T1
CHIP CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 10

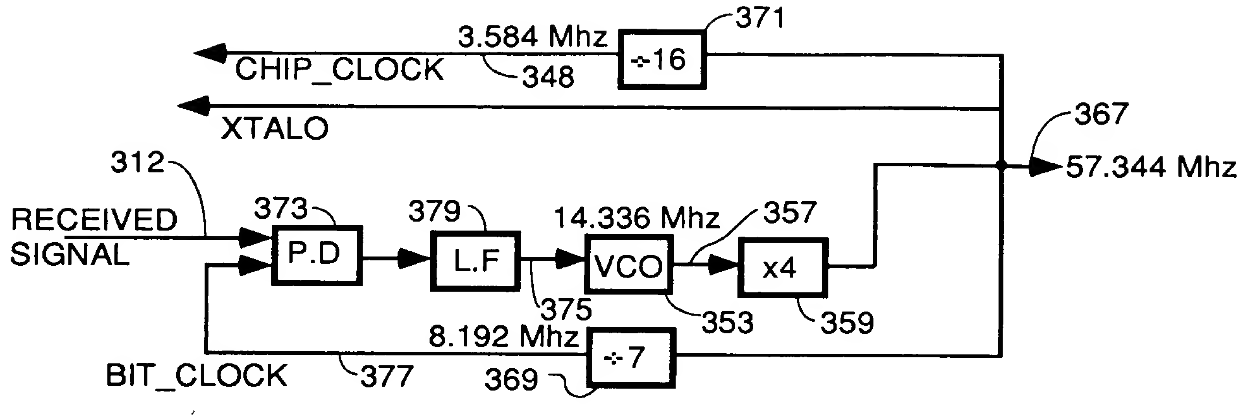


FIG. 11

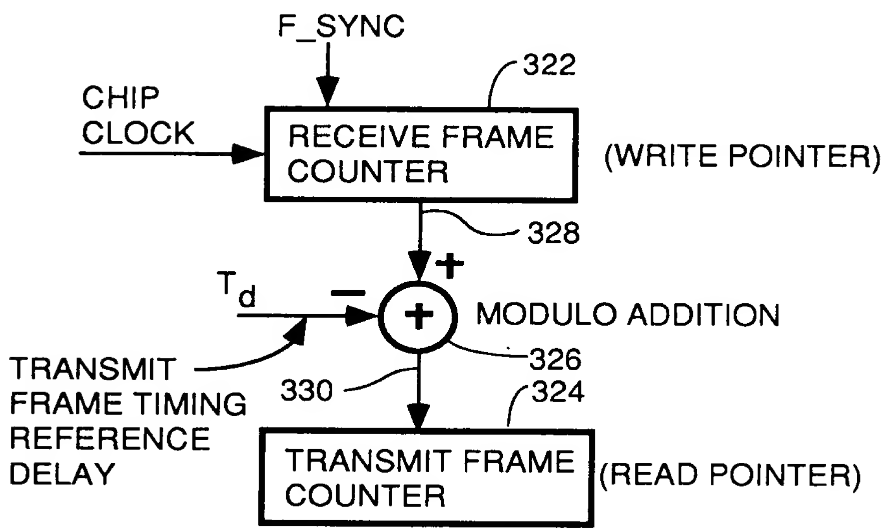


FIG. 12

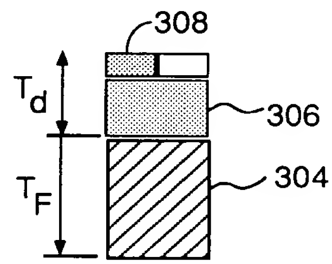


FIG. 13

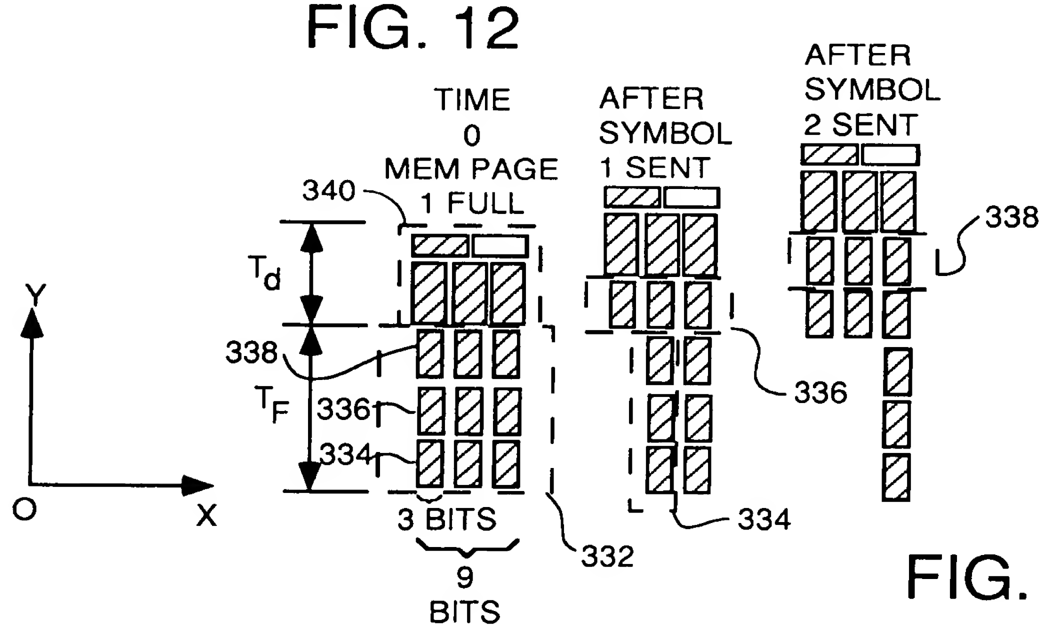


FIG. 14

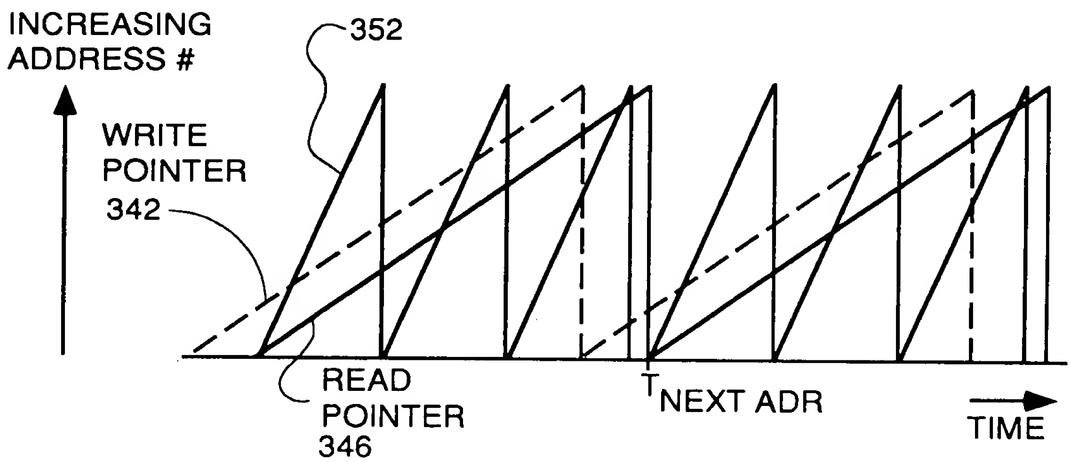

INCREASING
ADDRESS #
352
WRITE
POINTER
342
READ
POINTER
346
T
NEXT ADR
TIME

FIG. 15

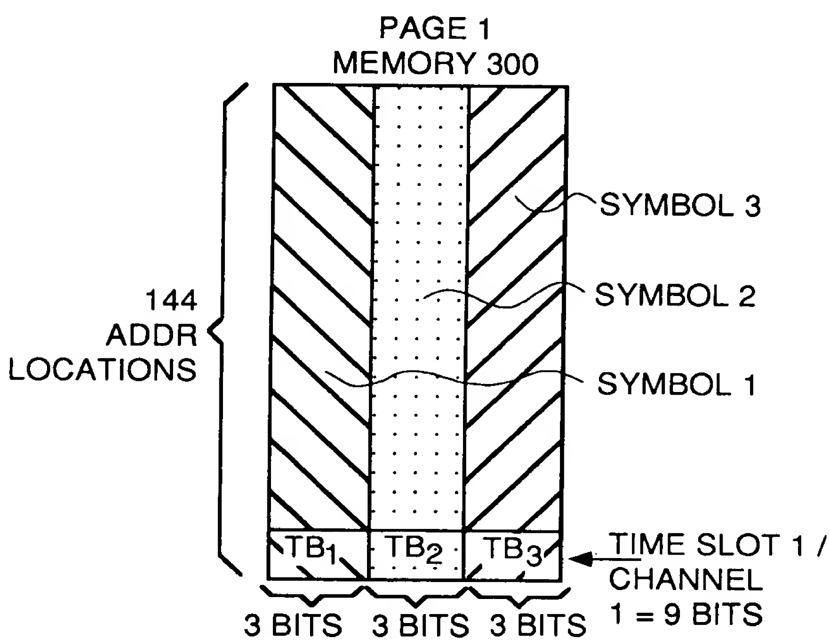
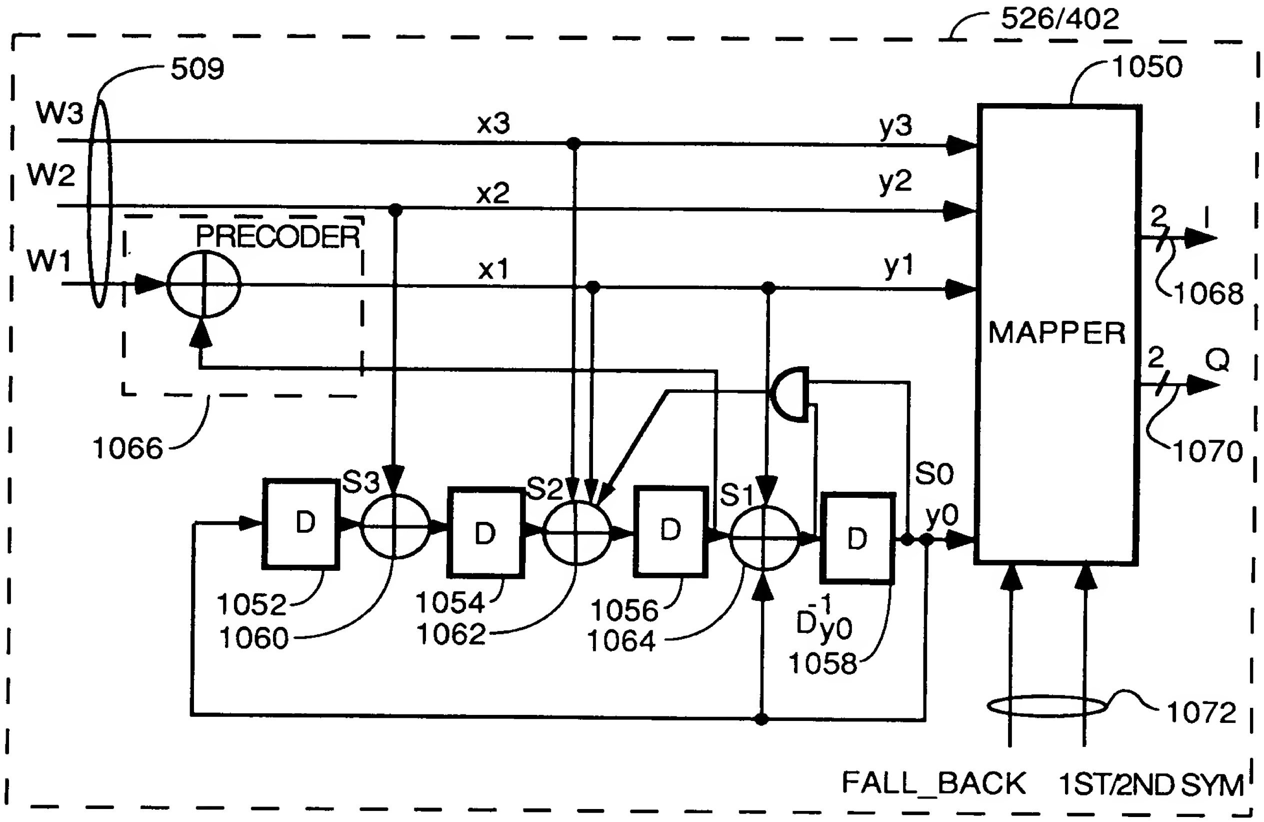

PAGE 1
MEMORY 300
SYMBOL 3
SYMBOL 2
SYMBOL 1
144
ADDR
LOCATIONS
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17

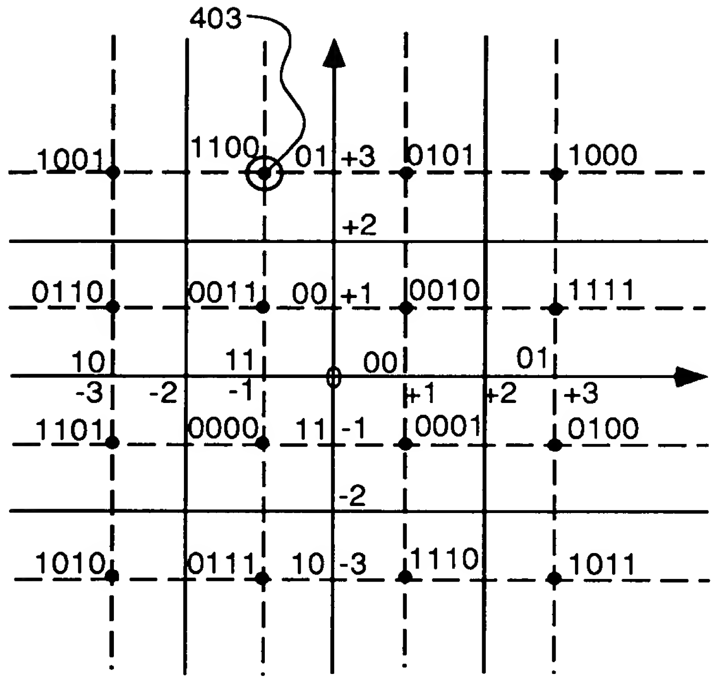


FIG. 18

403

0000	111	111	
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3∗ j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3∗ j
1000	011	011	=+3 + 3∗j
1001	101	011	= -3 + 3∗j
1010	101	101	= -3 - 3∗ j
1011	011	101	= 3 - 3∗ j
1100	111	011	= -1+ 3∗ j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3∗ j
1111	011	001	= 3 + j

FIG. 19

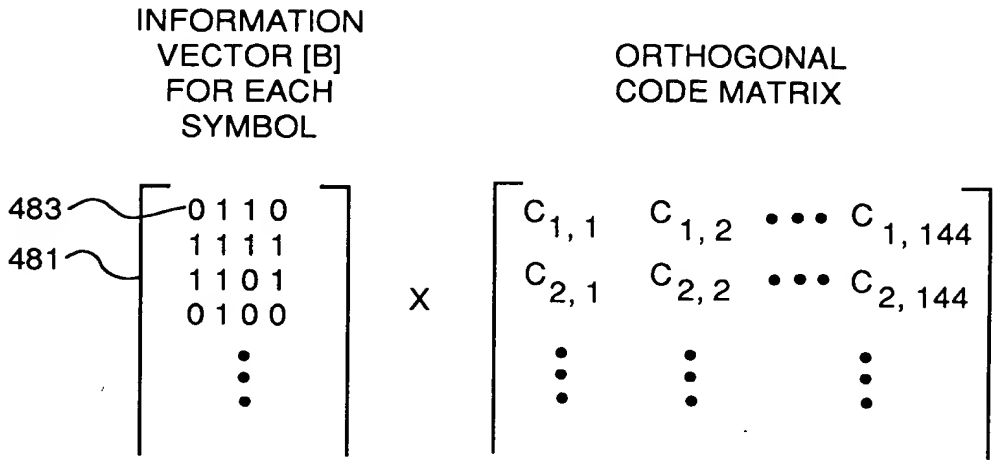


FIG. 20A

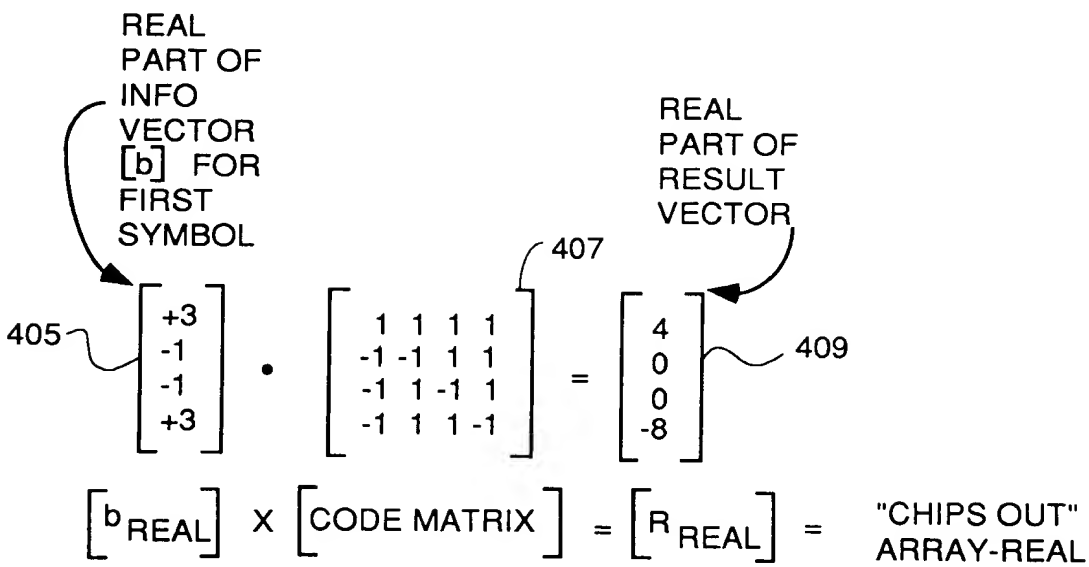


FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

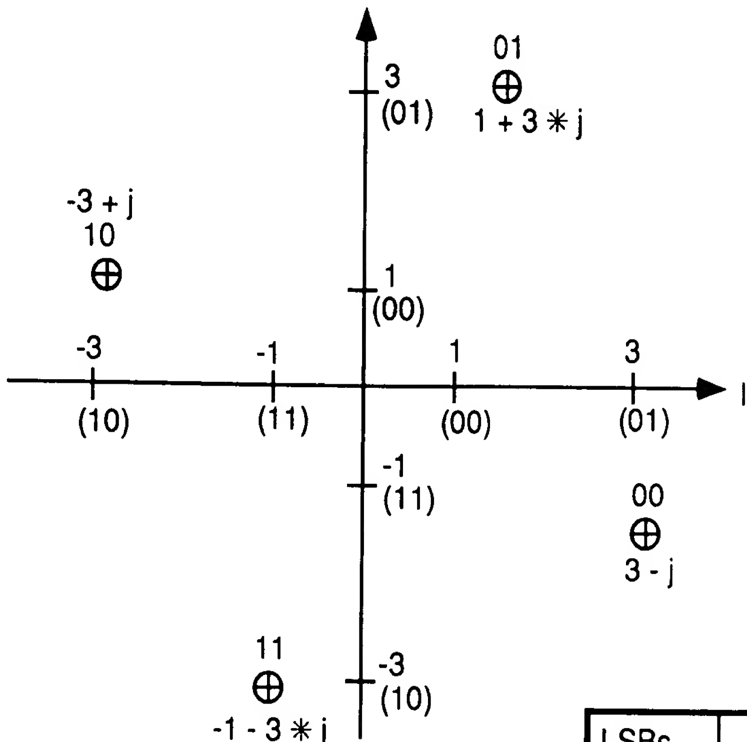


FIG. 21

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

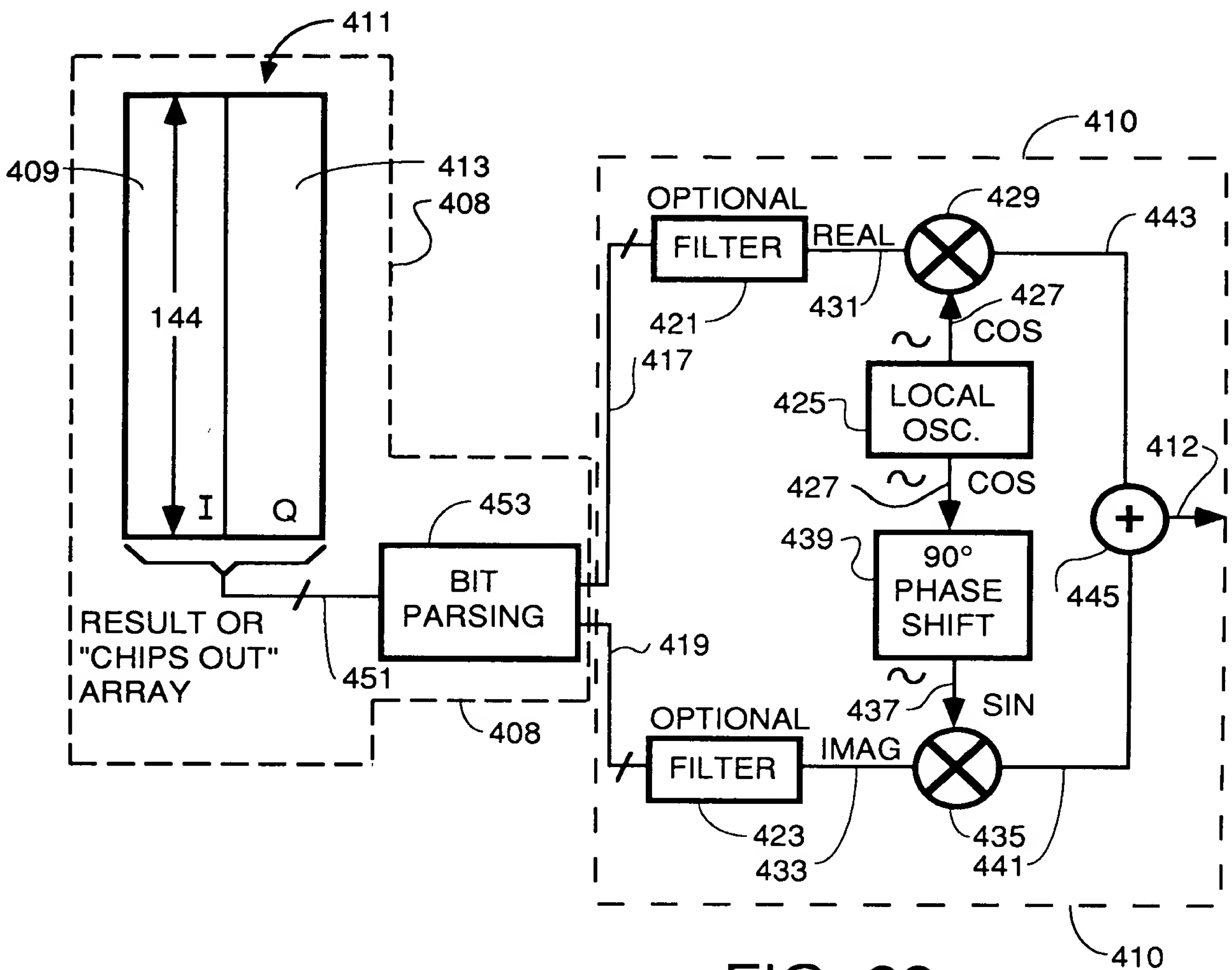

411
409
413
408
144
I
Q
RESULT OR
"CHIPS OUT"
ARRAY
451
453
BIT
PARSING
408
410
OPTIONAL
FILTER
REAL
429
443
431
427
COS
421
417
425
LOCAL
OSC.
427
COS
412
439
90°
PHASE
SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 23

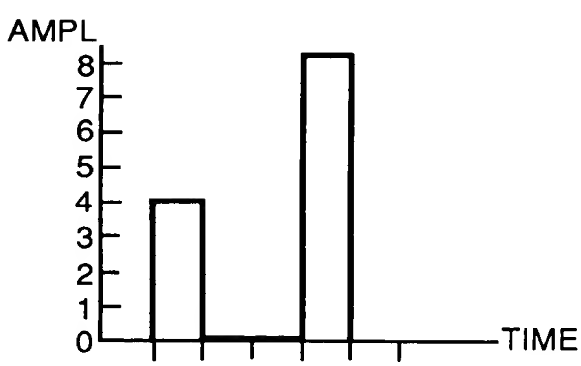

AMPL
8
7
6
5
4
3
2
1
0
TIME

FIG. 24

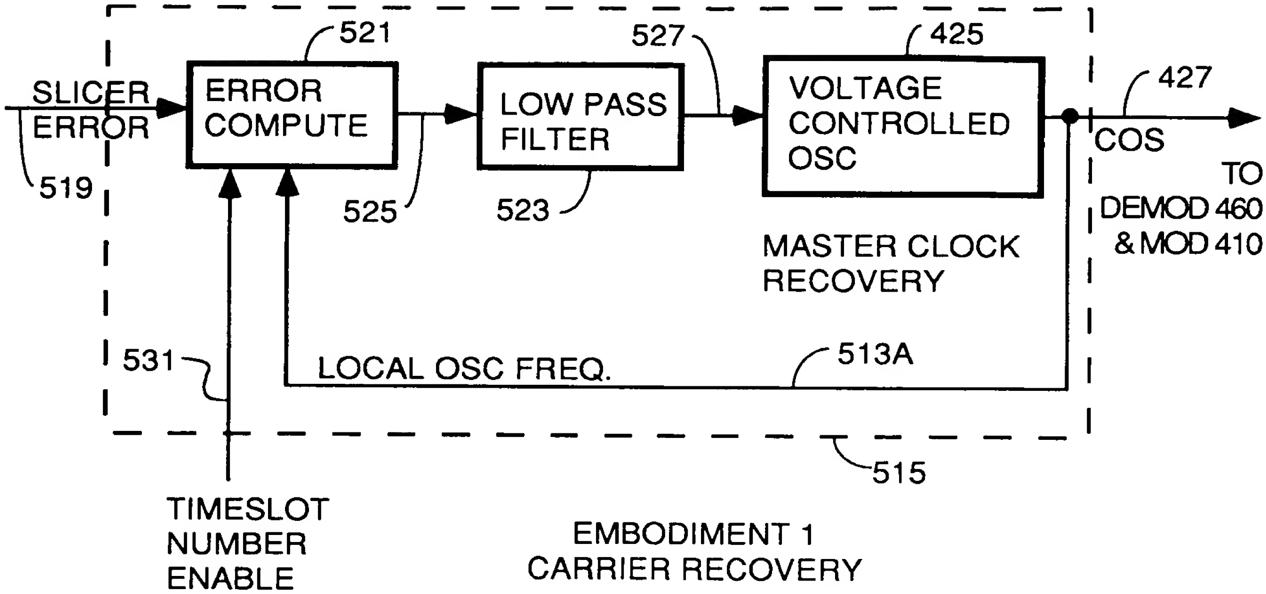

SLICER ERROR
519
521
ERROR COMPUTE
525
527
LOW PASS FILTER
523
425
VOLTAGE CONTROLLED OSC
427
COS
TO DEMOD 460 & MOD 410
MASTER CLOCK RECOVERY
531
LOCAL OSC FREQ.
513A
515
TIMESLOT NUMBER ENABLE
EMBODIMENT 1 CARRIER RECOVERY

FIG. 25

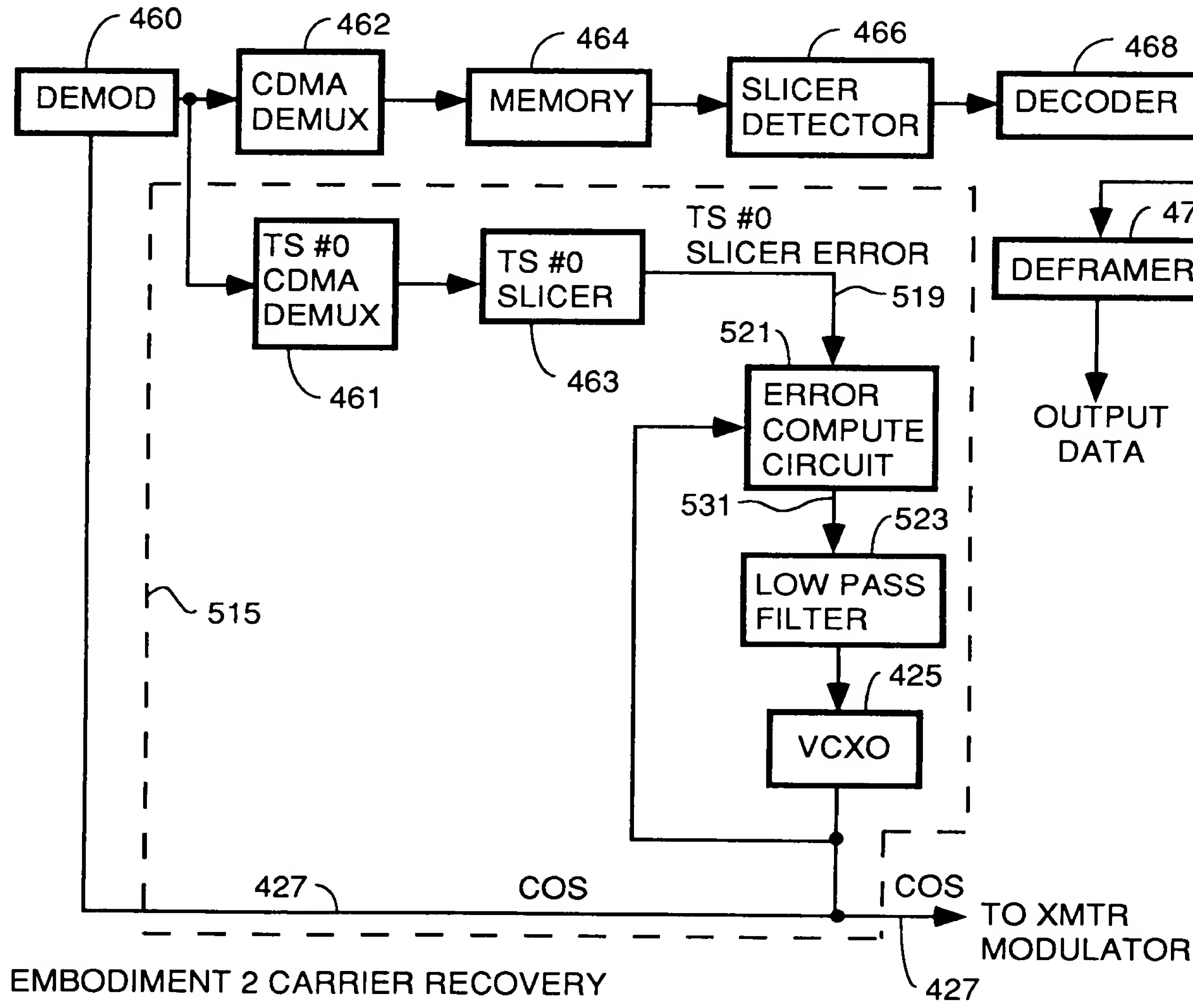

460
DEMOD
462
CDMA DEMUX
464
MEMORY
466
SLICER DETECTOR
468
DECODER
470
DEFRAMER
OUTPUT DATA
TS #0 CDMA DEMUX
461
TS #0 SLICER
463
TS #0 SLICER ERROR
519
521
ERROR COMPUTE CIRCUIT
531
523
LOW PASS FILTER
425
VCXO
515
427
COS
COS
TO XMTR MODULATOR
427
EMBODIMENT 2 CARRIER RECOVERY

FIG. 26

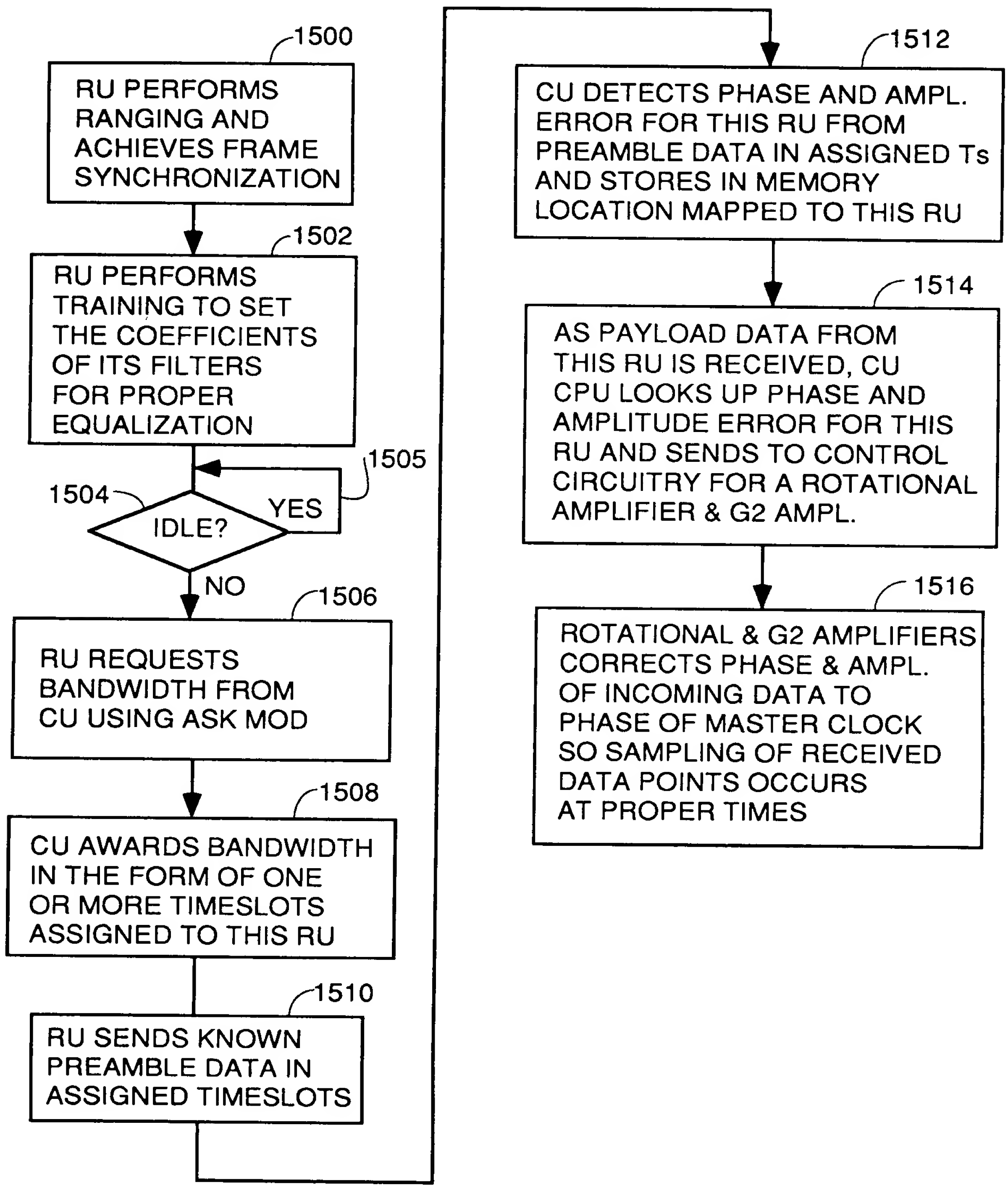
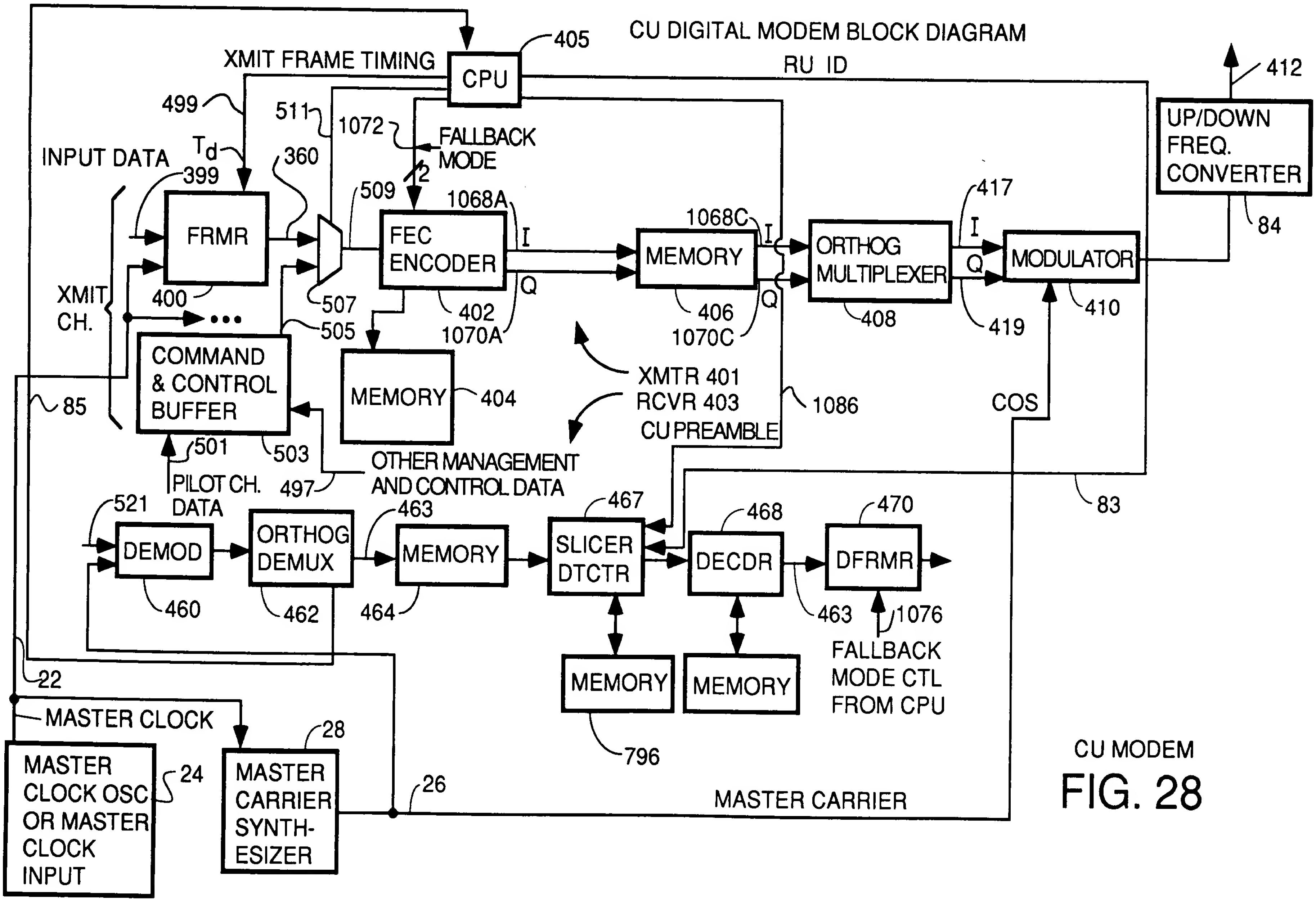

1500
RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1502
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1504
IDLE?
YES
1505
NO
1506
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1508
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1510
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1512
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED Ts AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1514
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1516
ROTATIONAL & G2 AMPLIFIERS CORRECTS PHASE & AMPL. OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES

FIG. 27



CU MODEM

FIG. 28

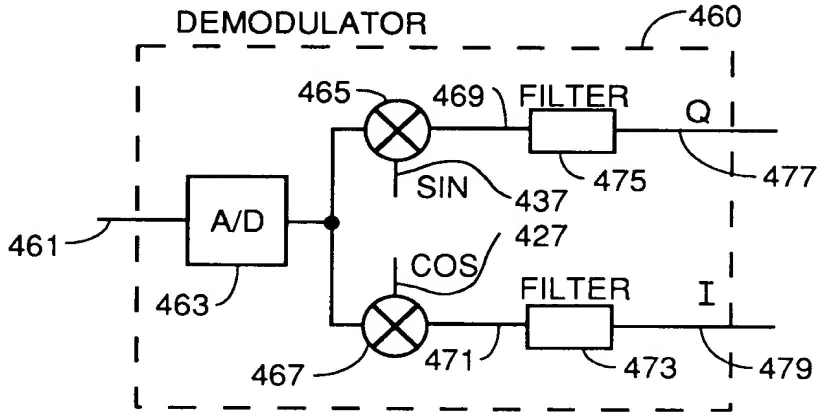
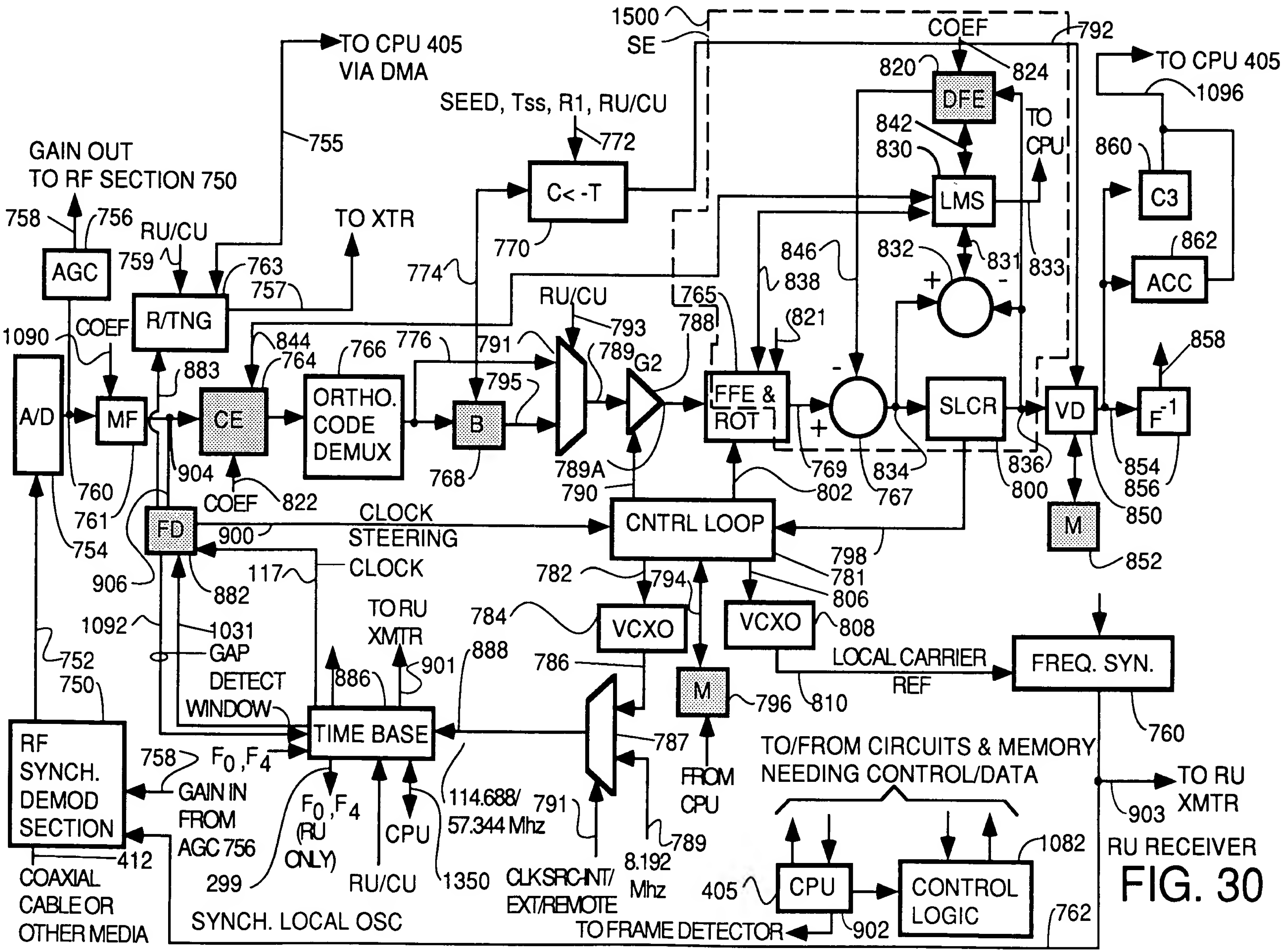
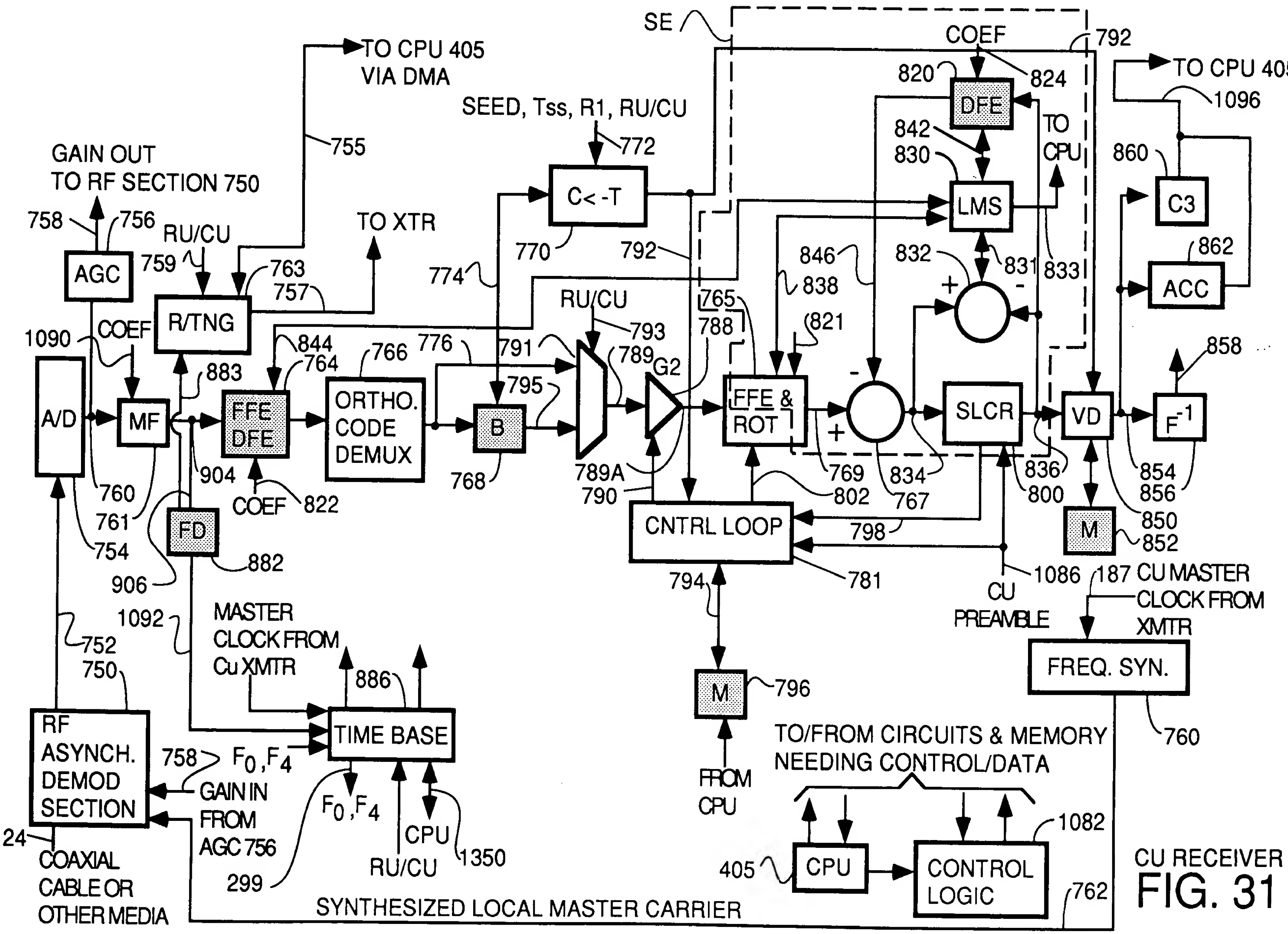

DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
A/D
461
463
427
COS
FILTER
I
467
471
473
479

FIG. 29

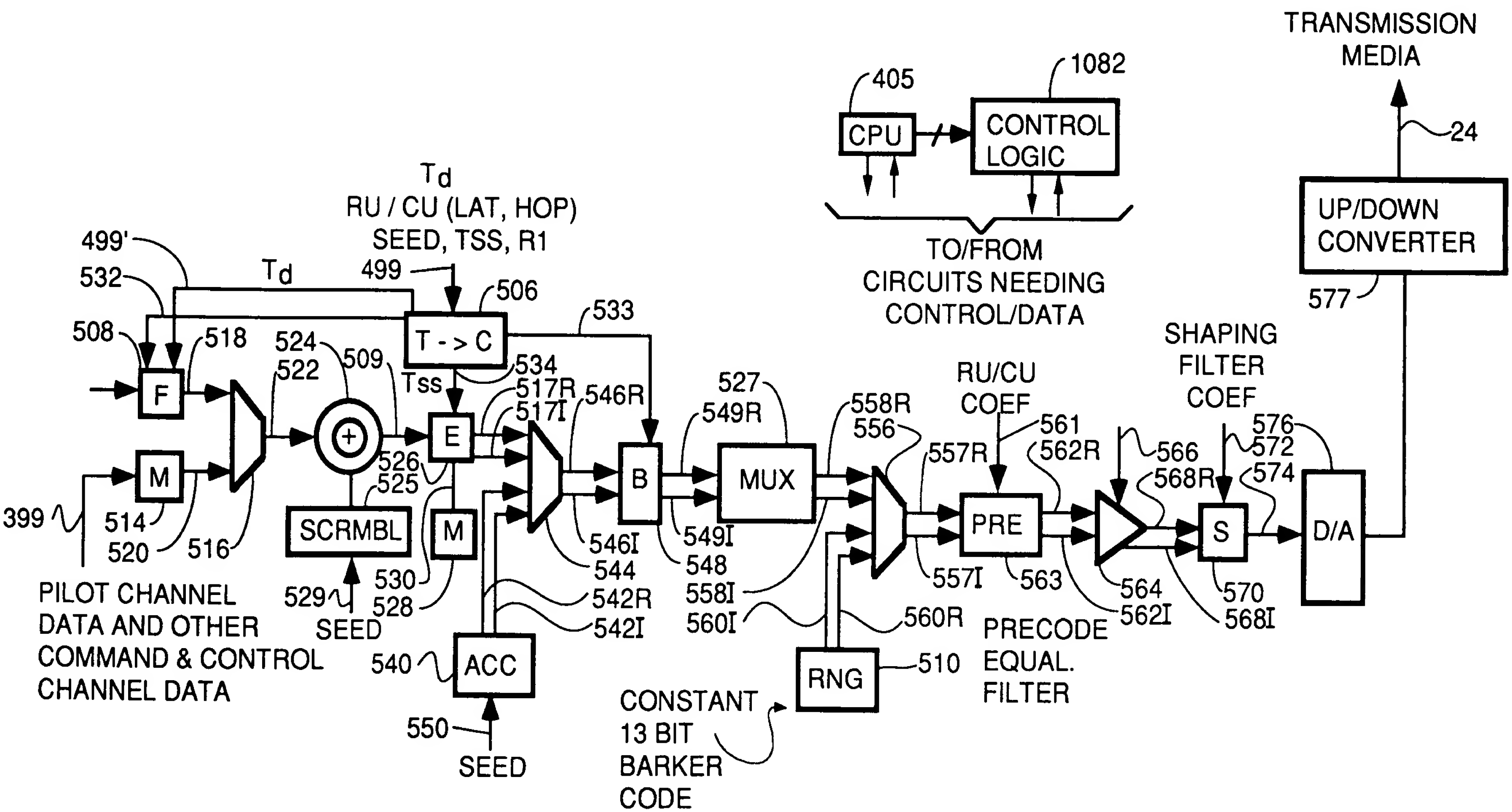


RU RECEIVER

FIG. 30

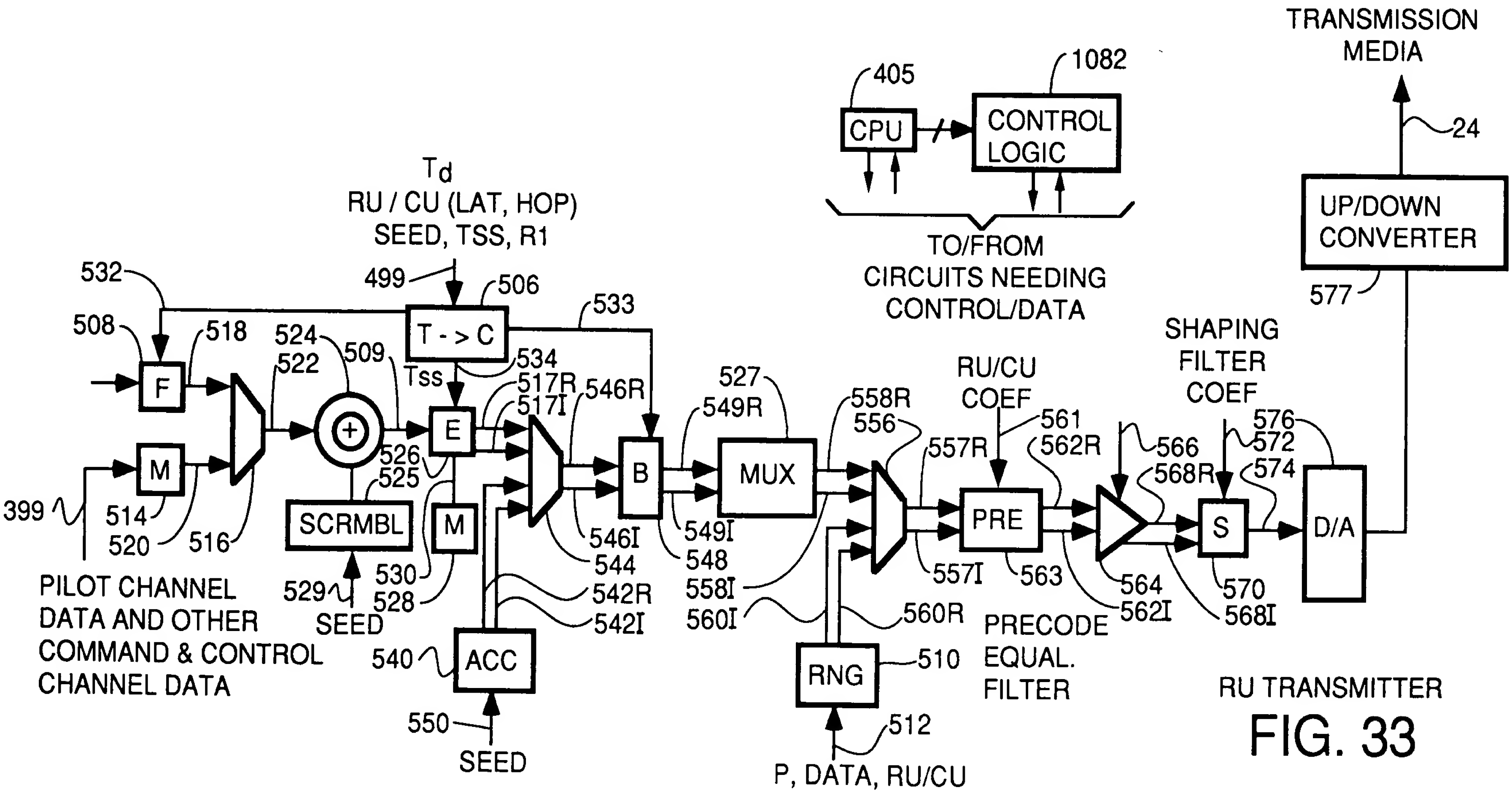


CU RECEIVER
FIG. 31



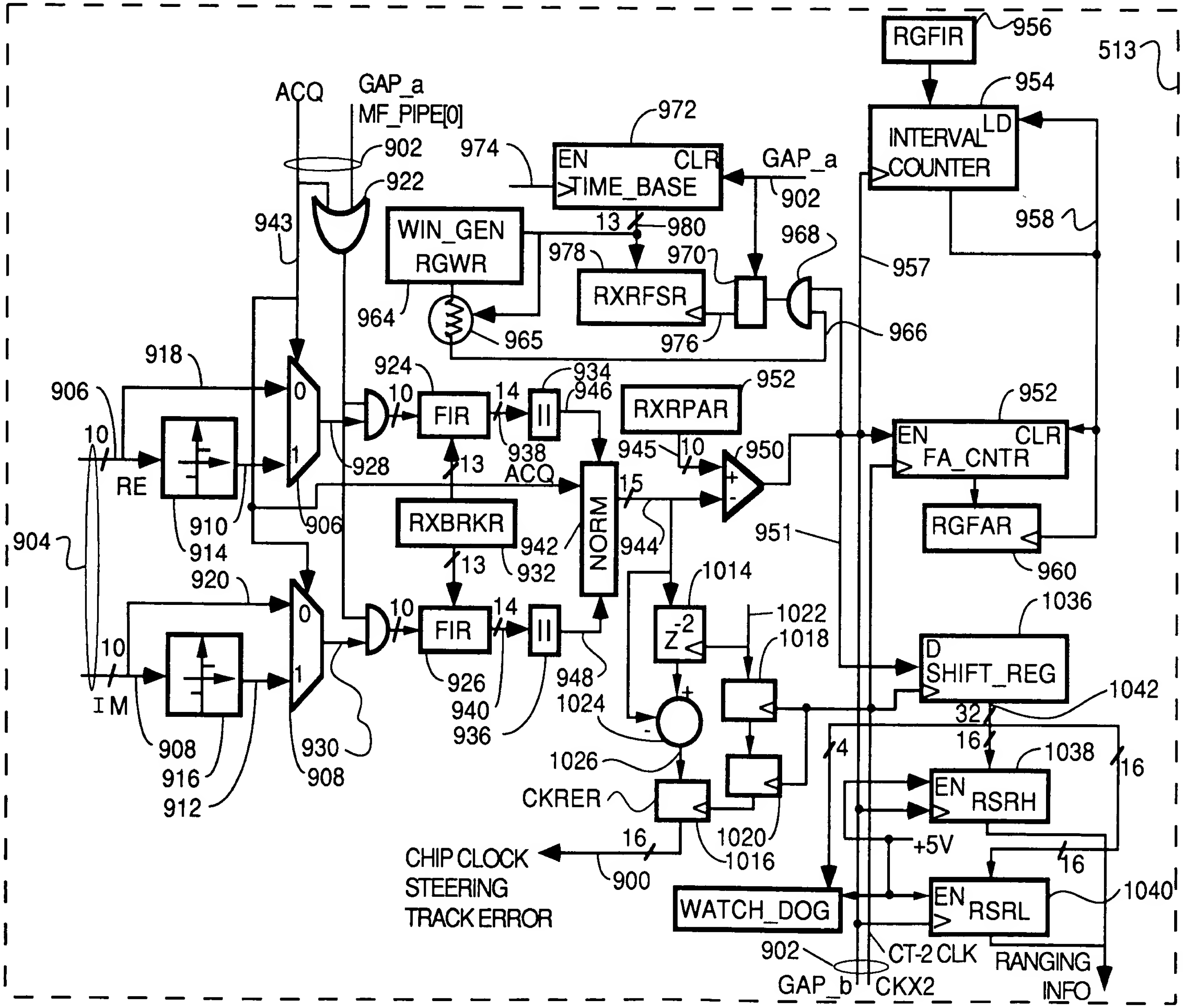
CU TRANSMITTER

FIG. 32



RU TRANSMITTER

FIG. 33



FRAME DETECTOR/ RANGING DETECTOR

FIG. 34

GAP ACQUISITION TIMING

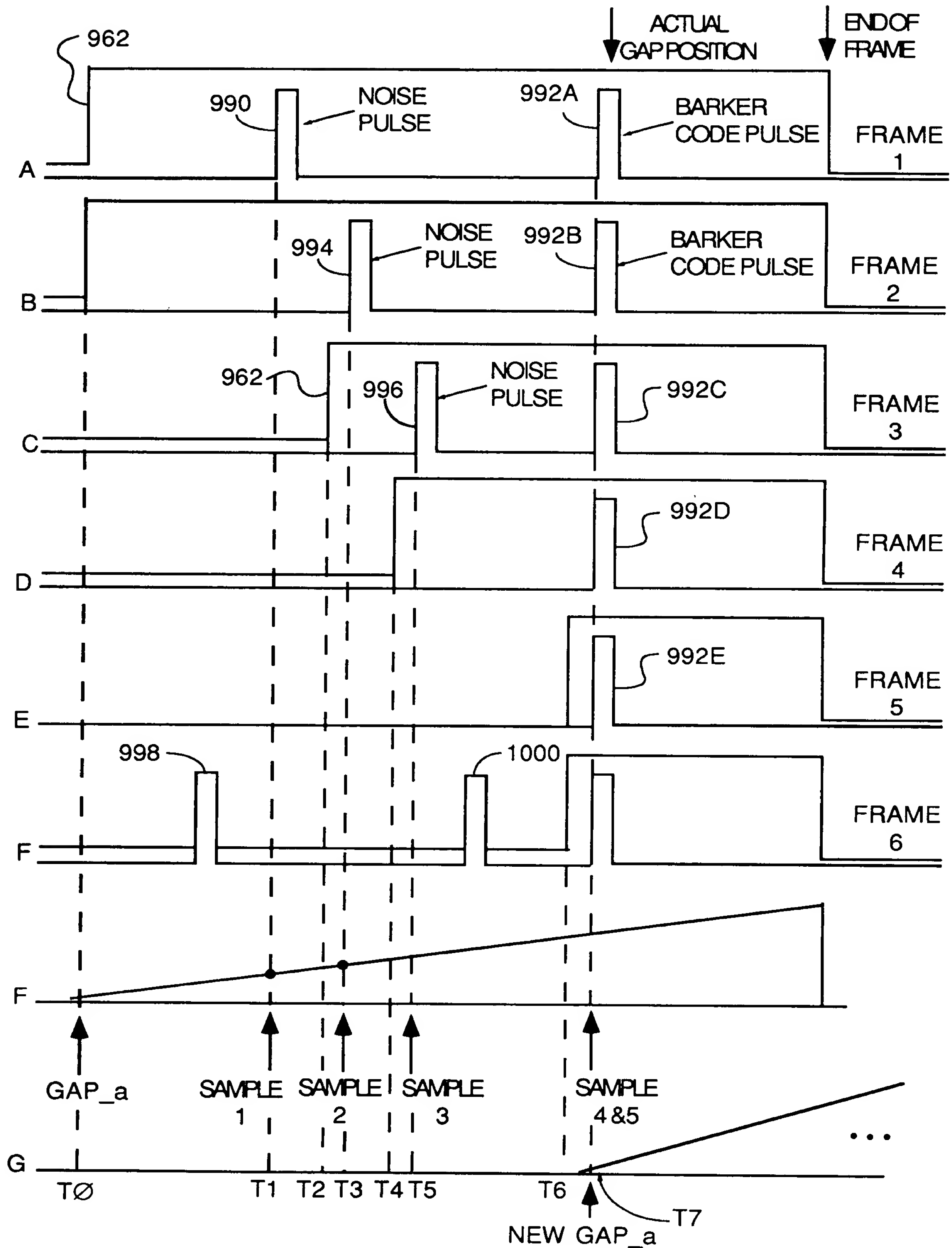


FIG. 35

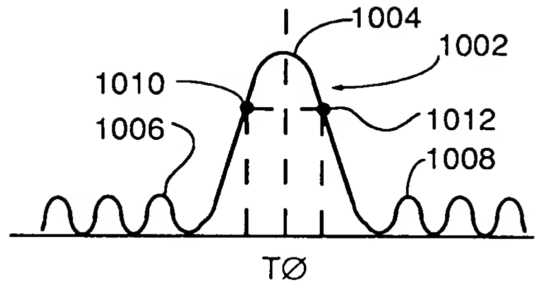


FIG. 36

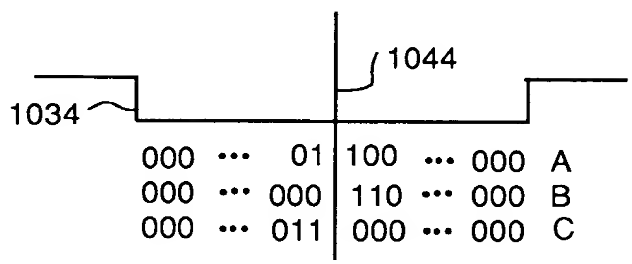


FIG. 37
FINE TUNING TO
CENTER BARKER CODE

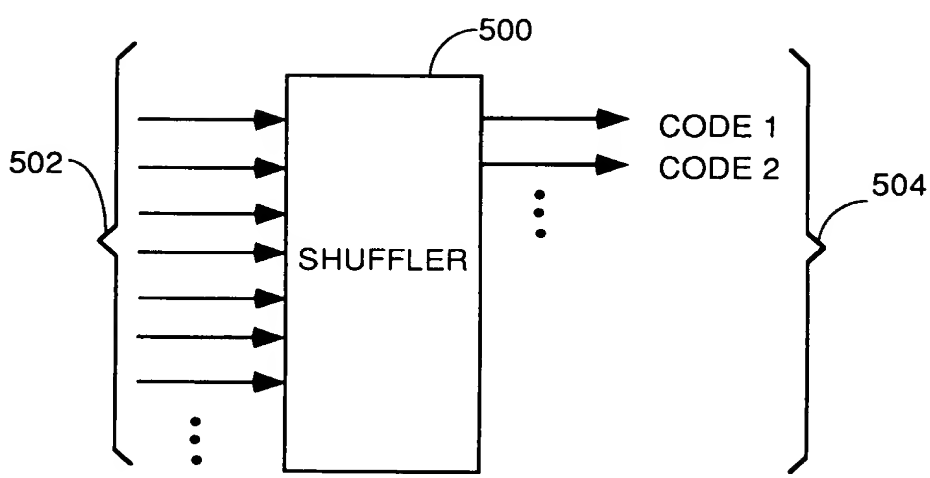


FIG. 38

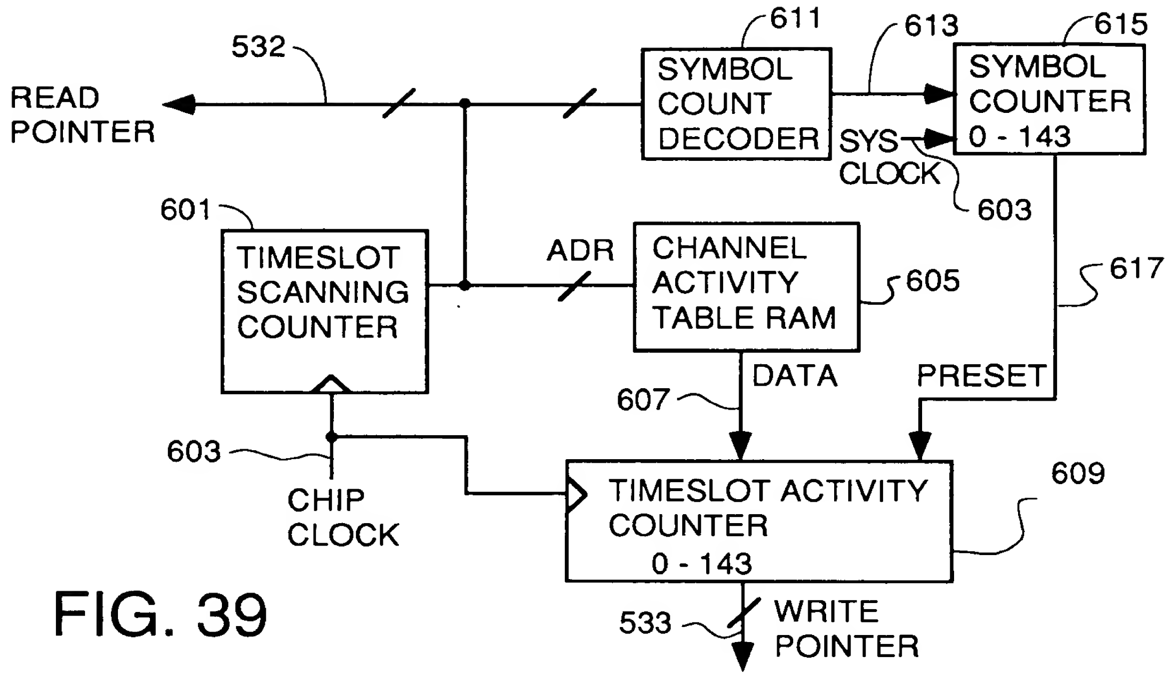


FIG. 39

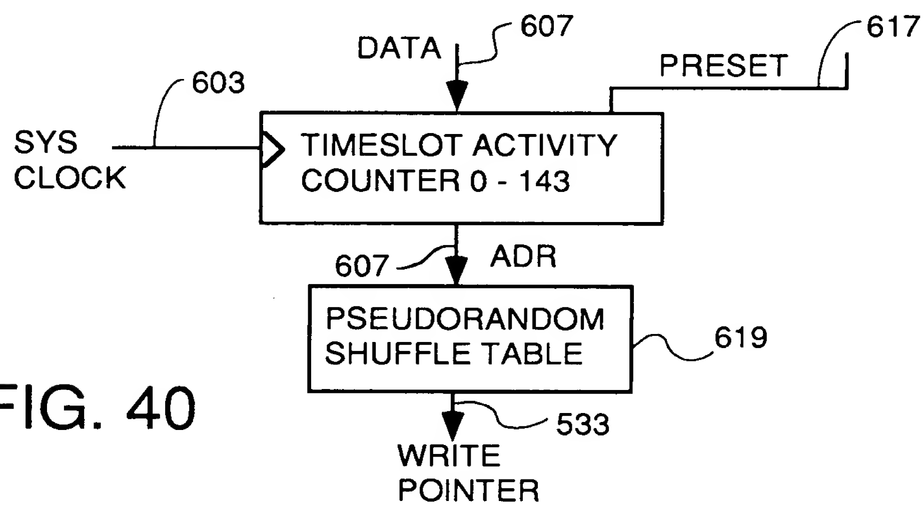


FIG. 40

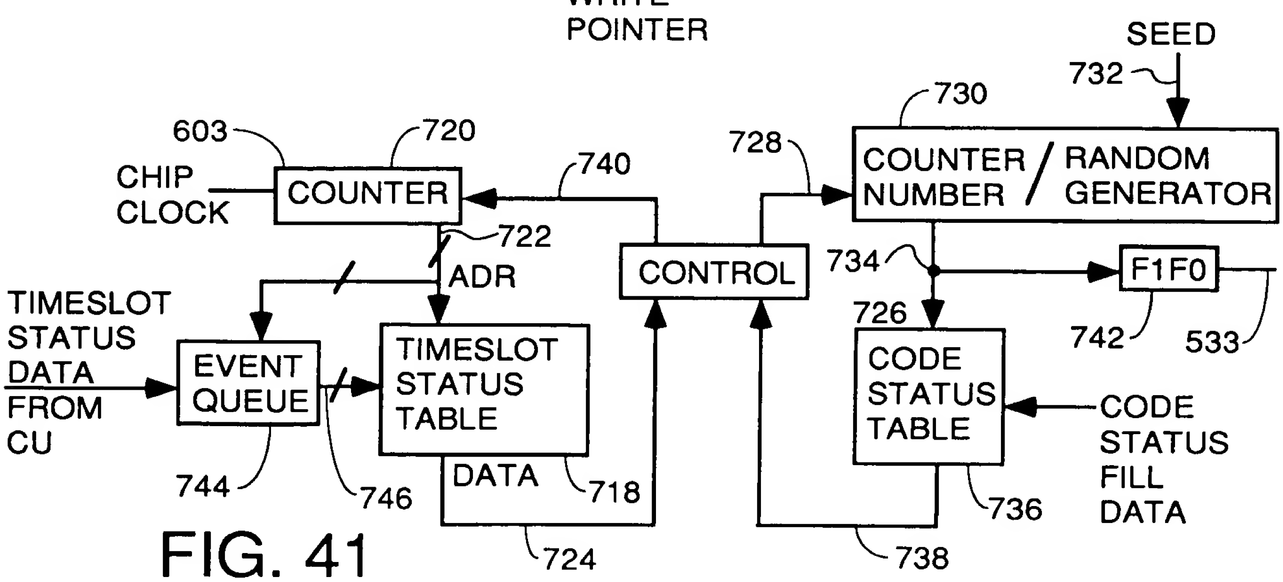


FIG. 41

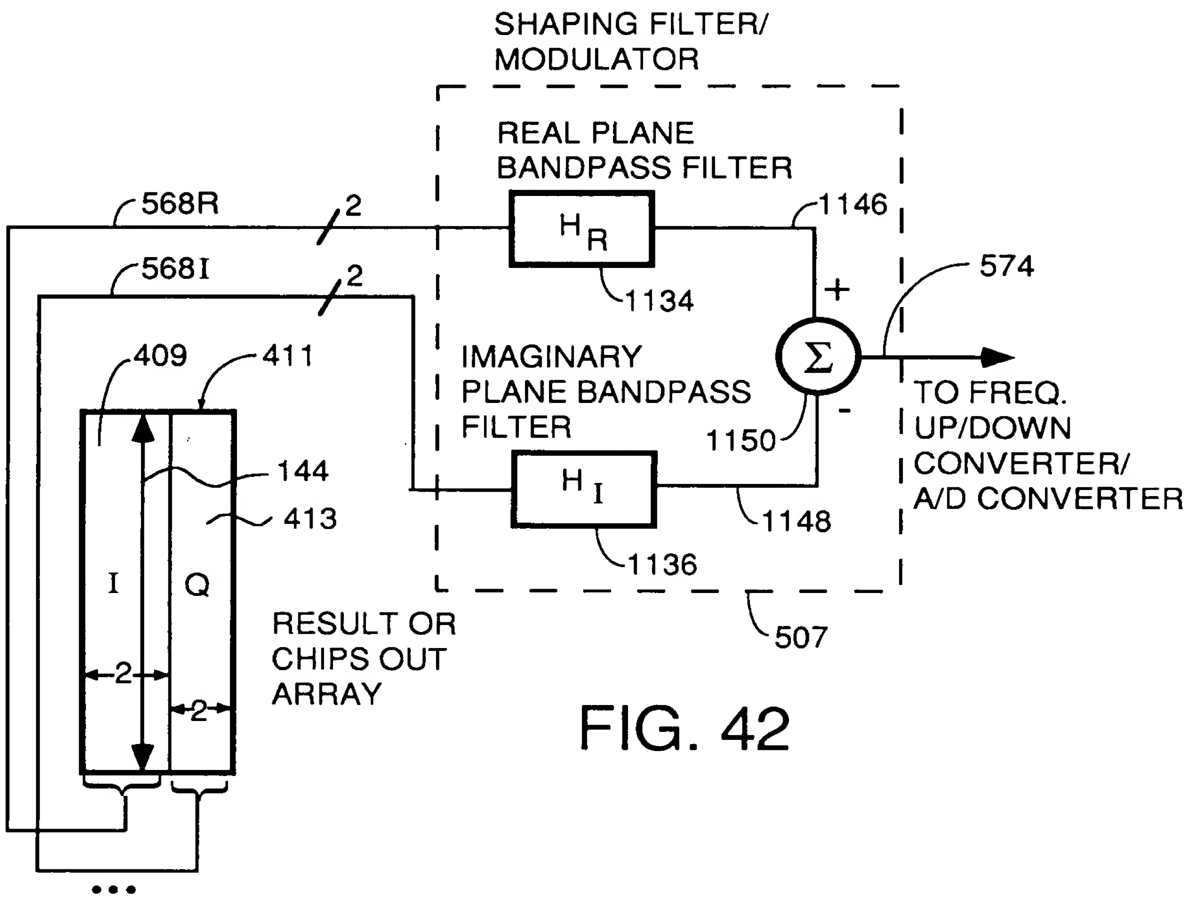


FIG. 42

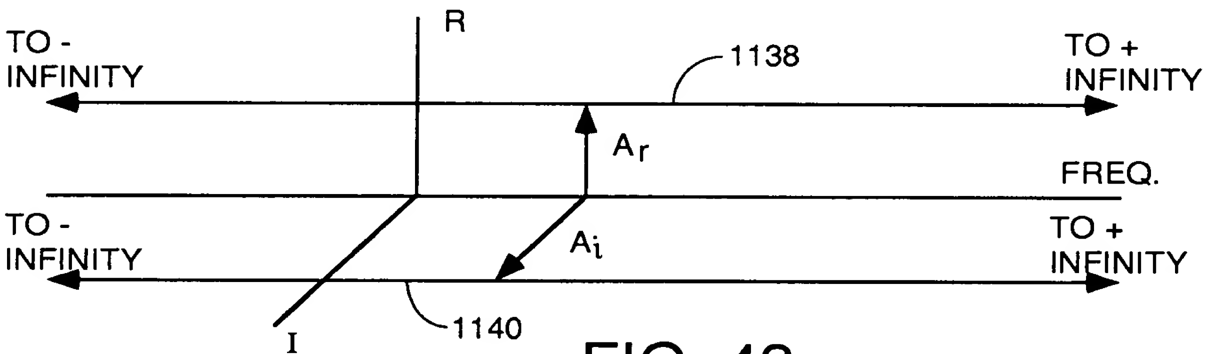


FIG. 43

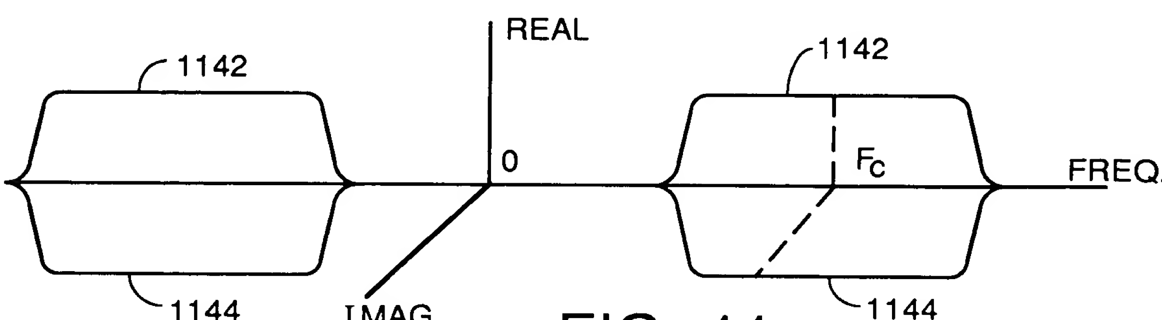
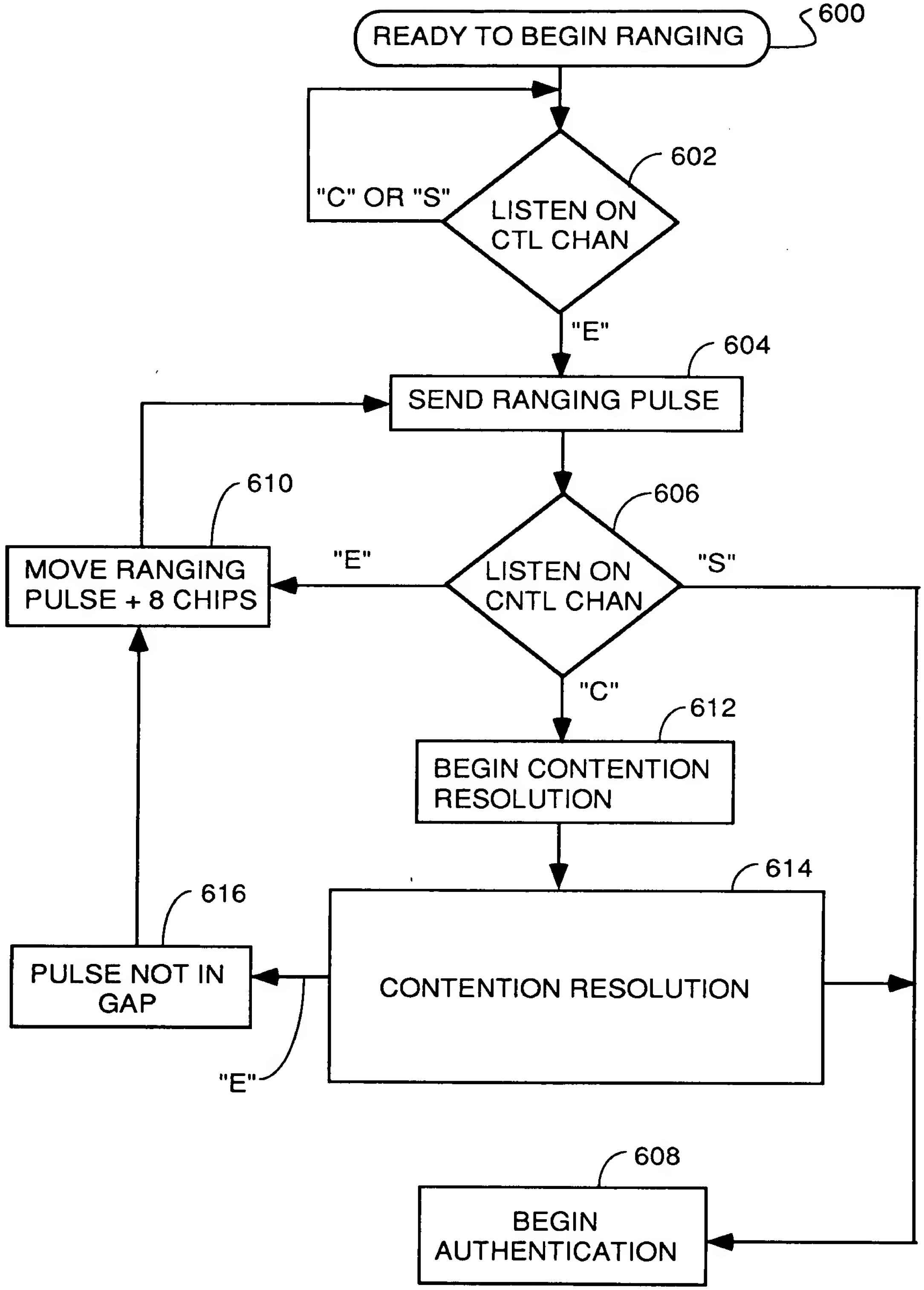
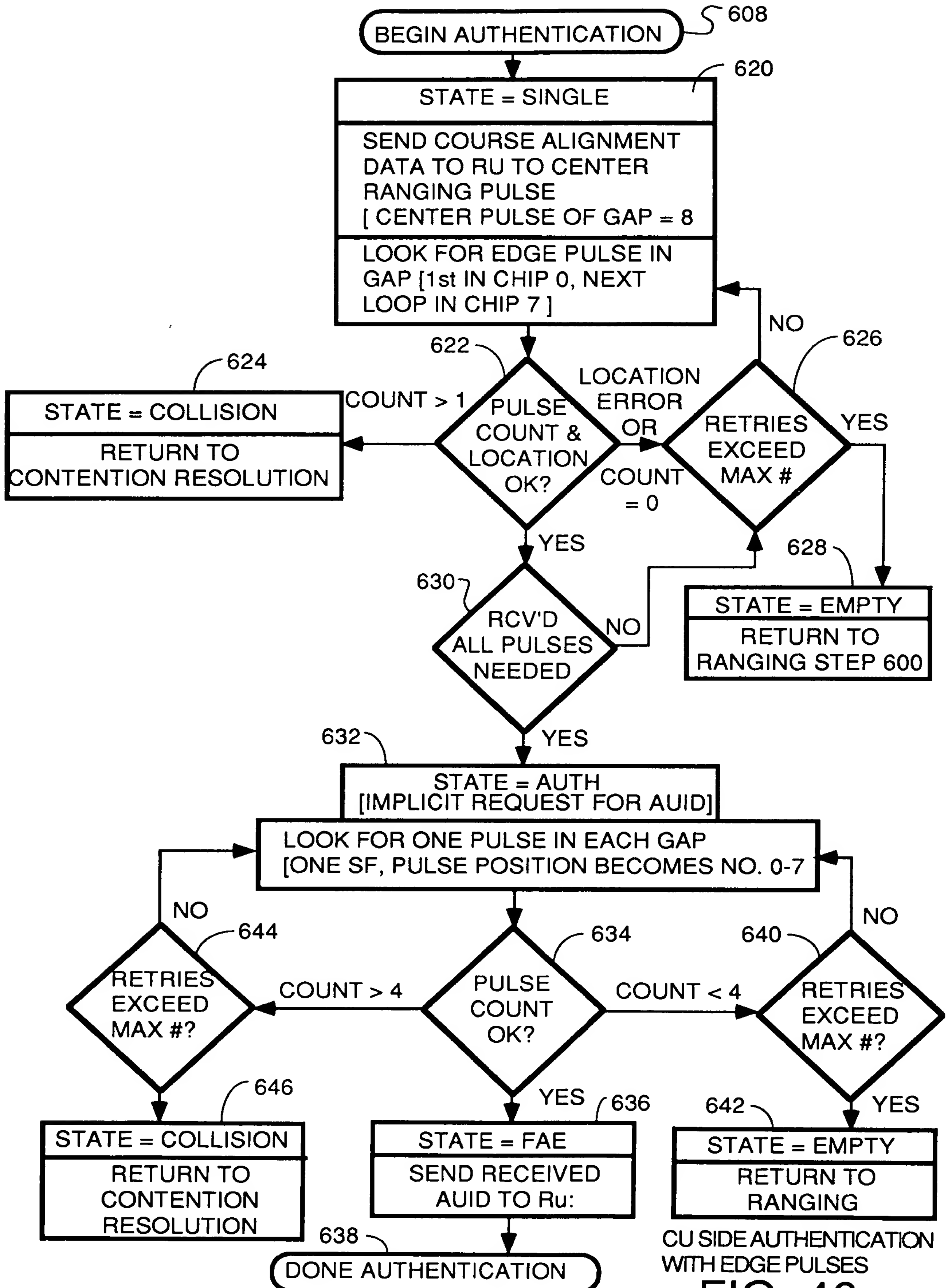


FIG. 44



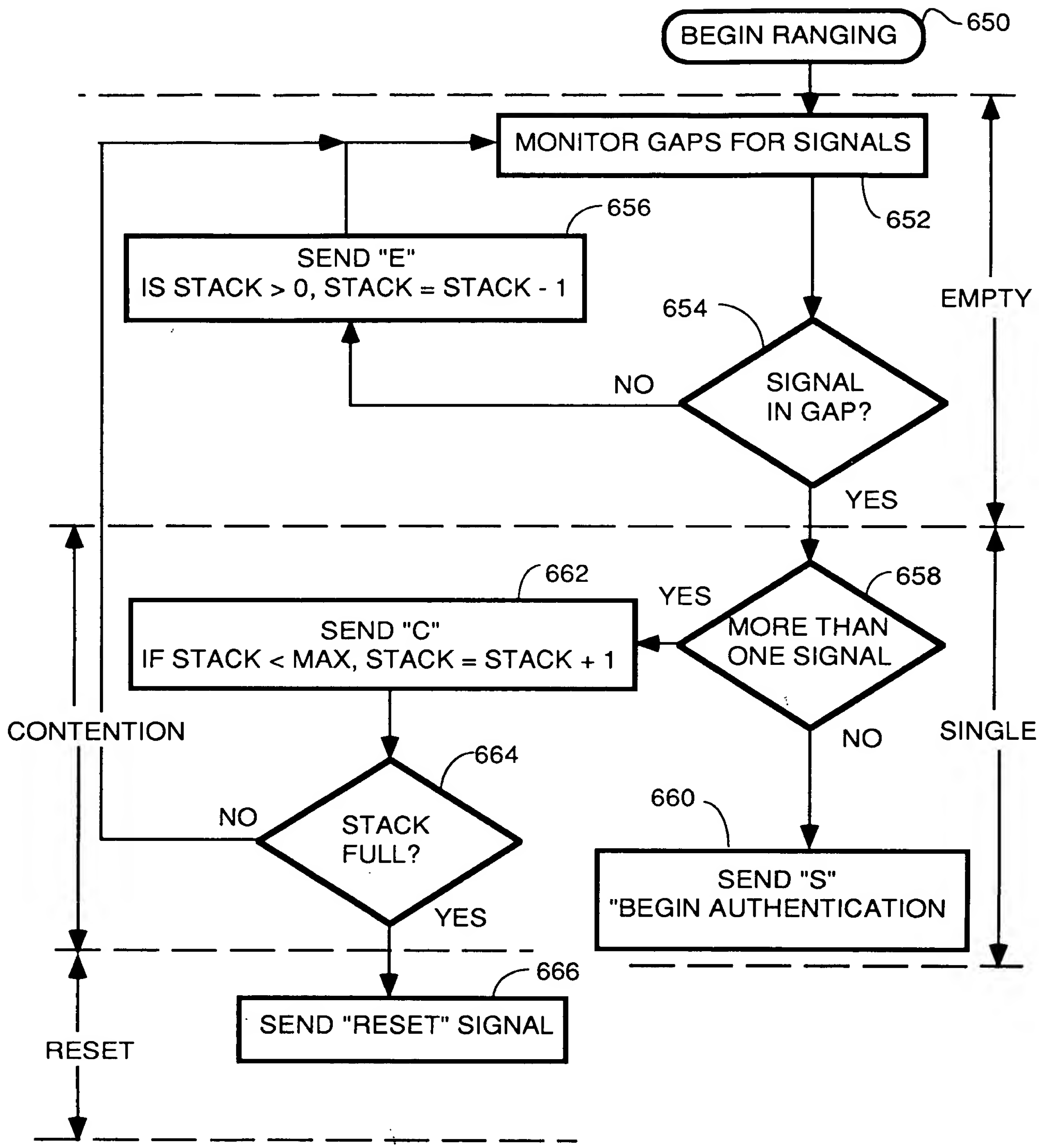
RU RANGING

FIG. 45



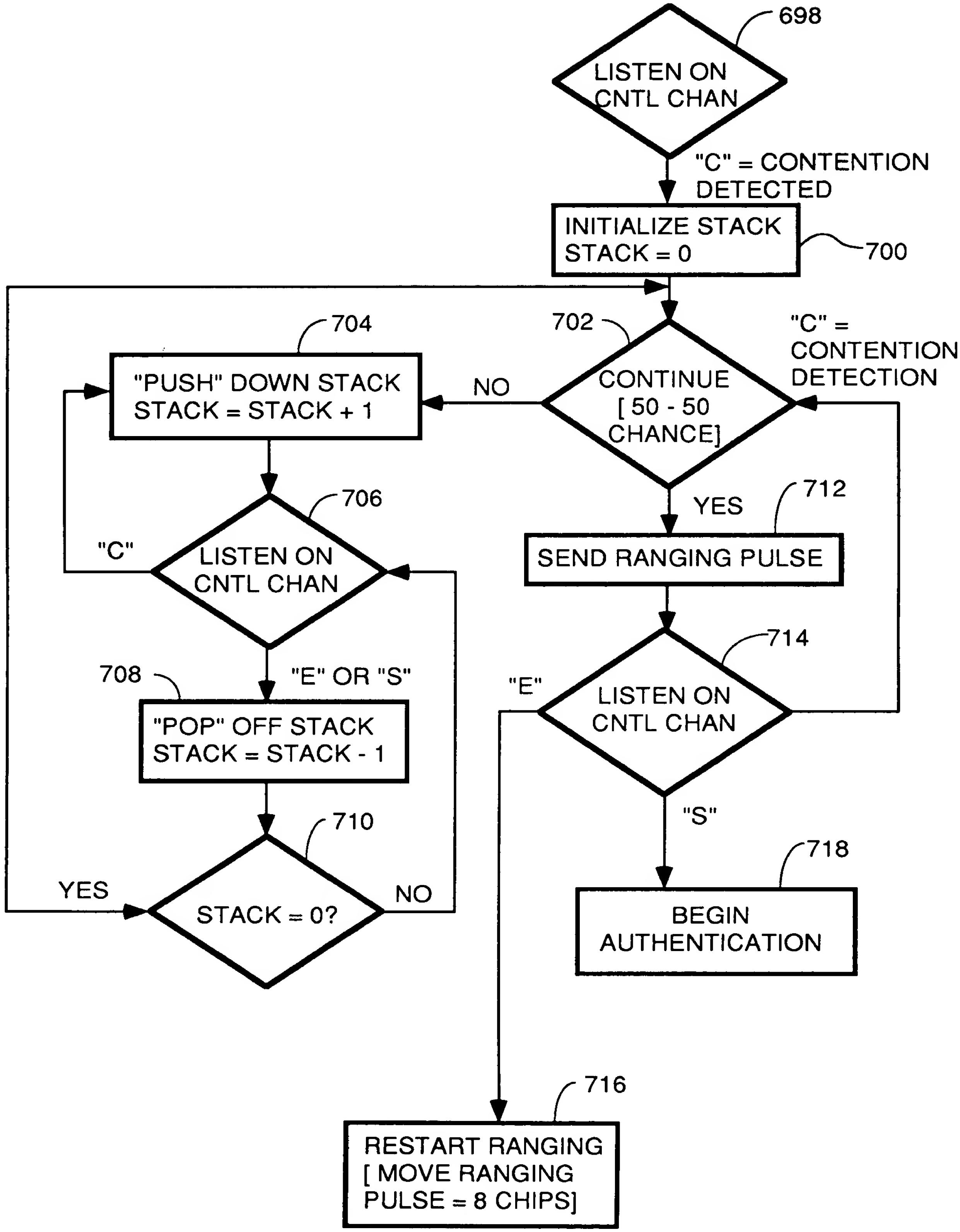
CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 46



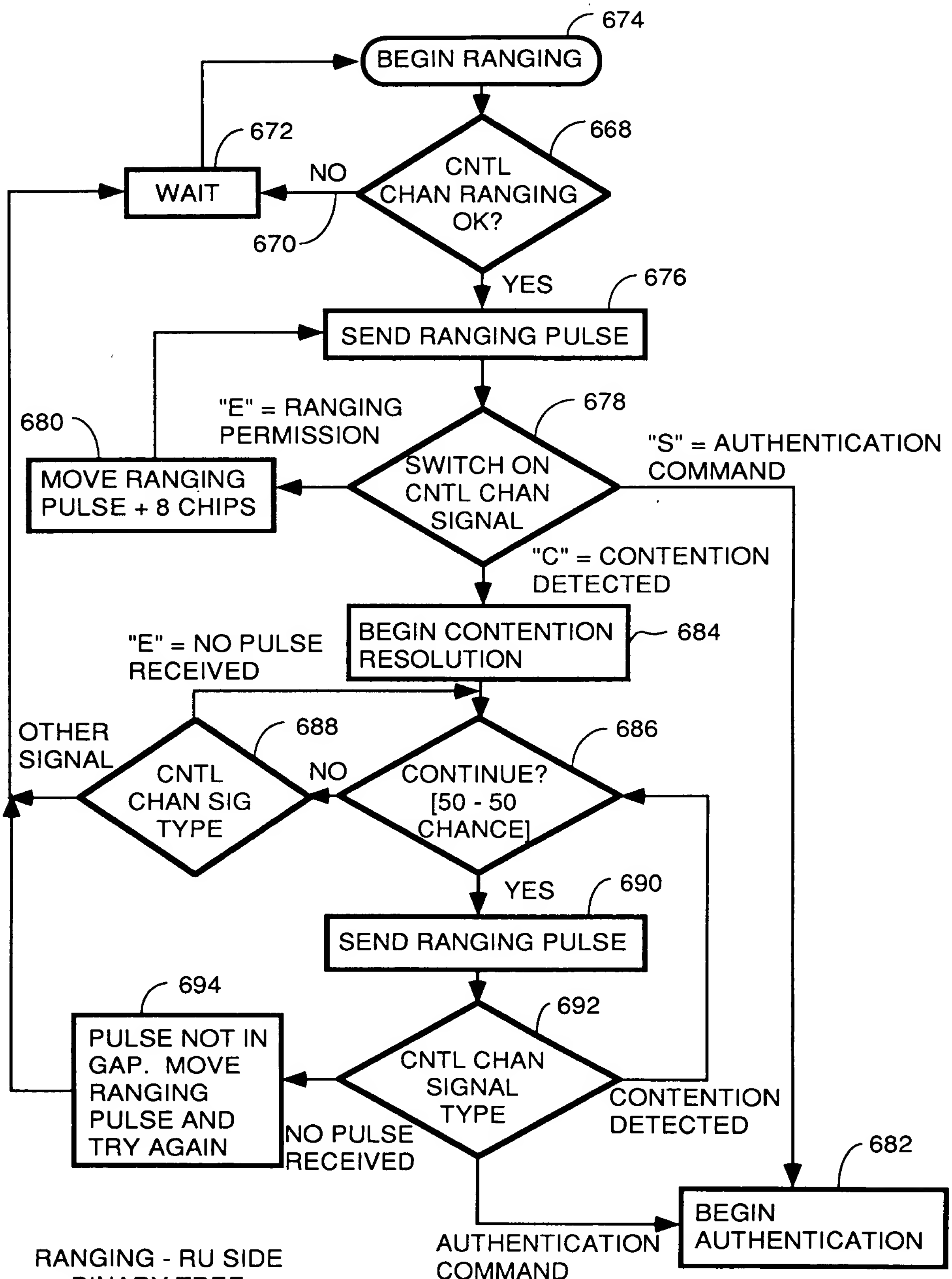
CU RANGING AND CONTENTION RESOLUTION

FIG. 47



CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 48



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 49

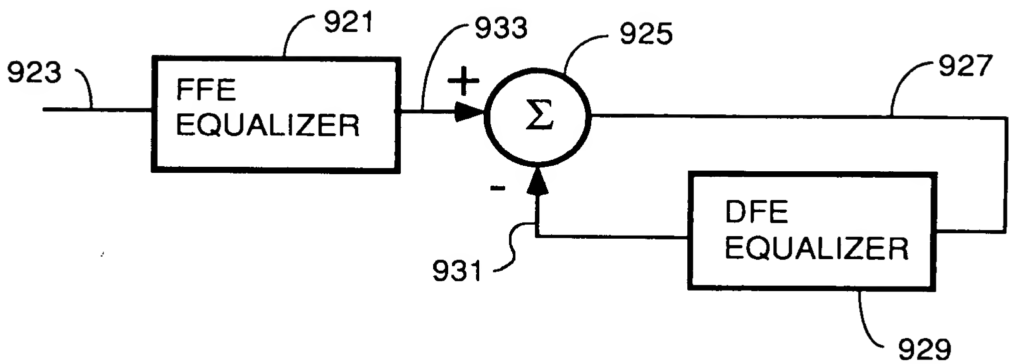
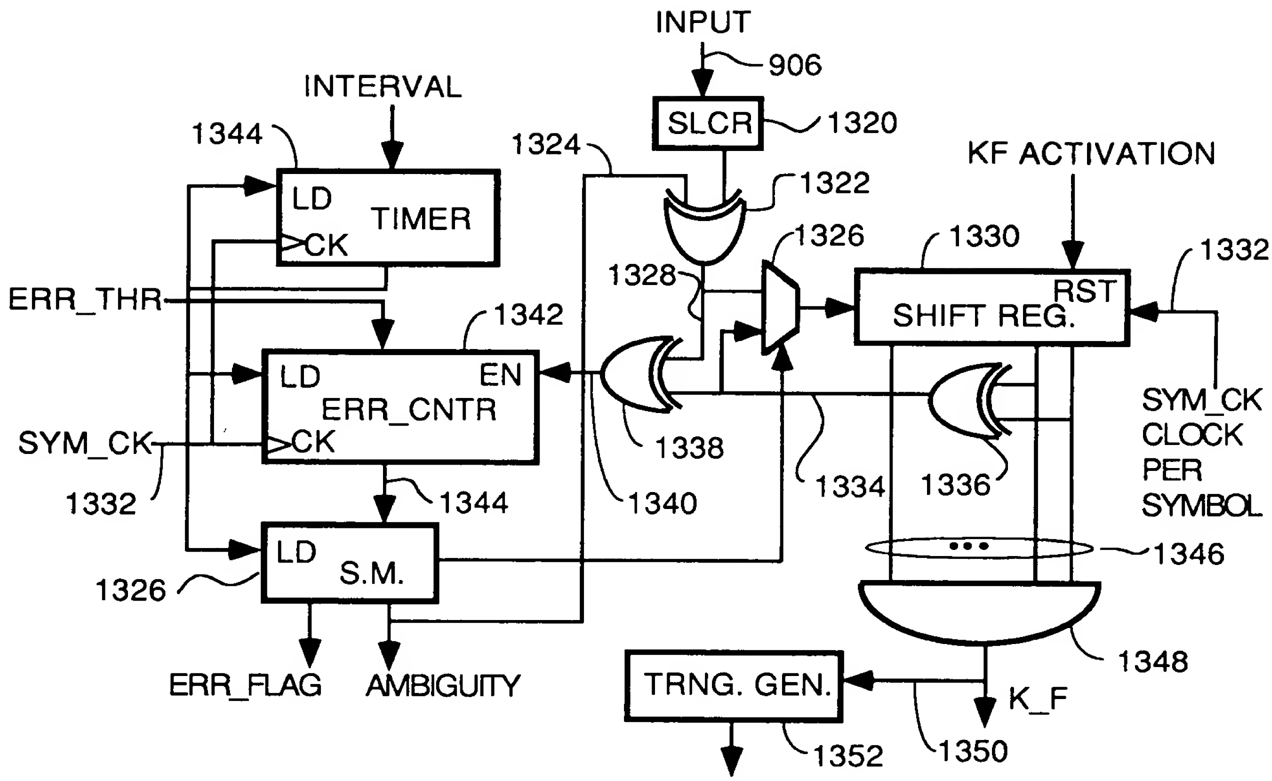
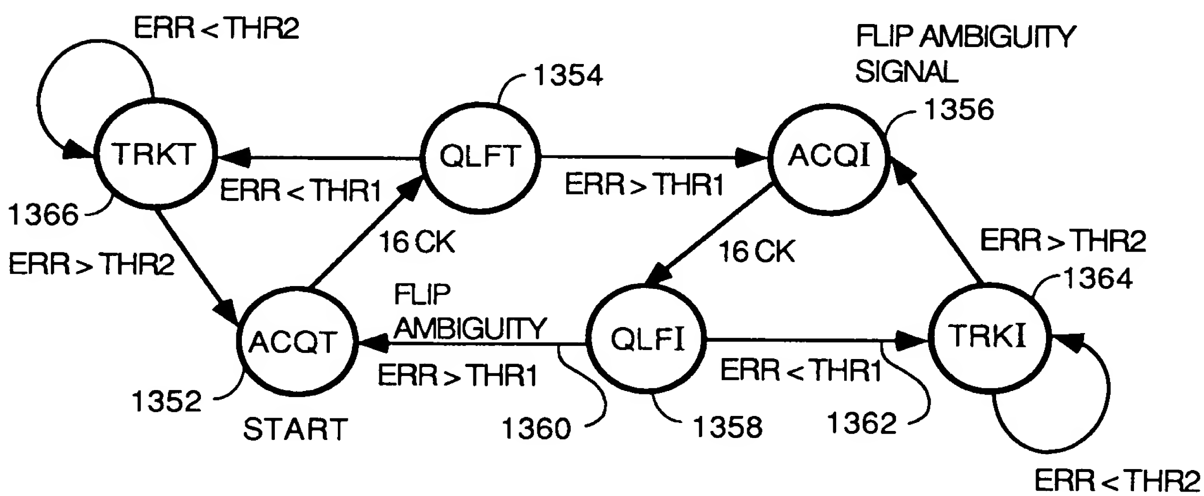


FIG. 50



FRAME DETECTOR
FRAME SYNC/KILOFRAME DETECT

FIG. 51



STATE MACHINE

FIG. 52

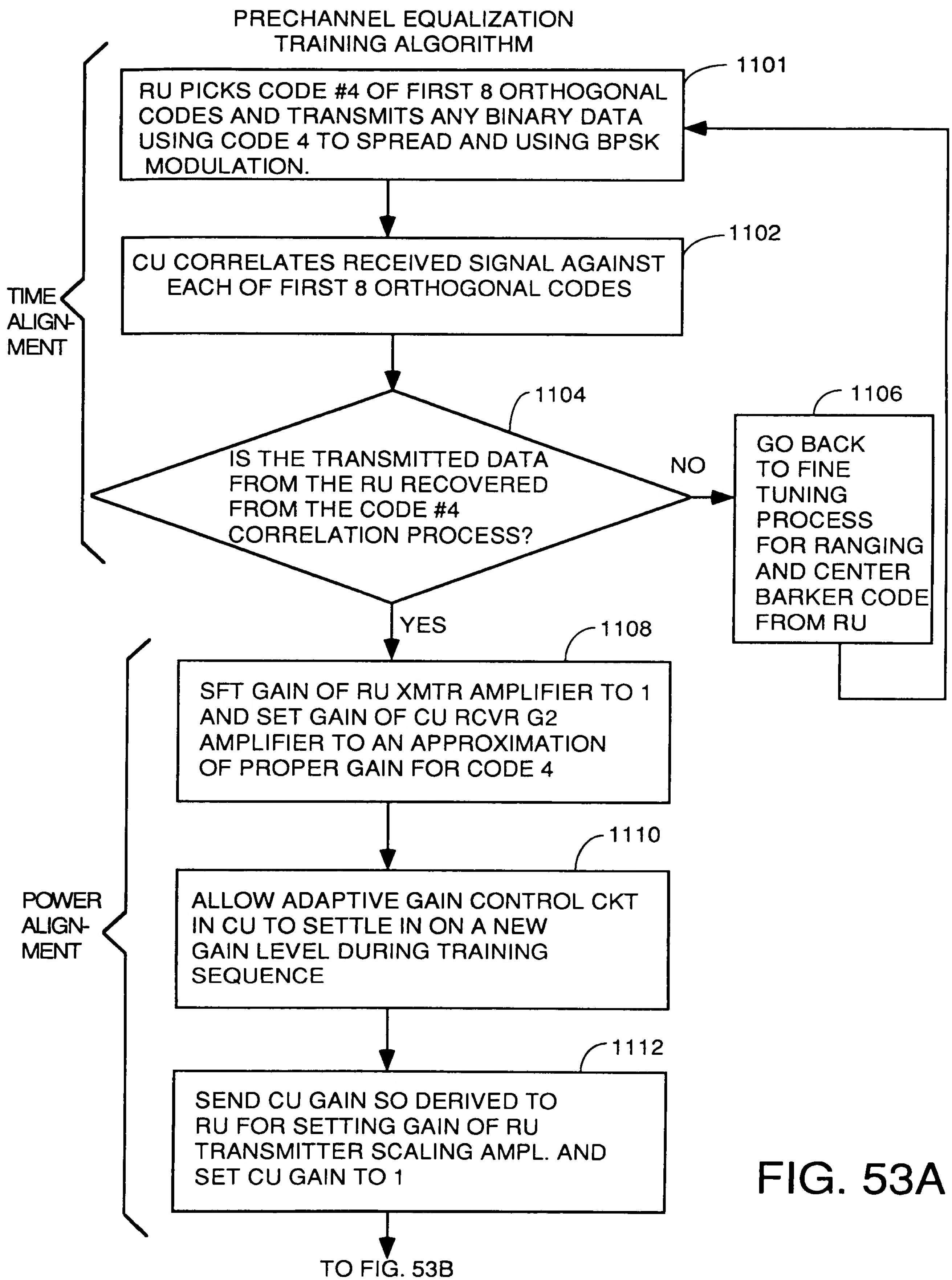

PRECHANNEL EQUALIZATION
TRAINING ALGORITHM
1101
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGN-MENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
POWER ALIGN-MENT
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 53B

FIG. 53A

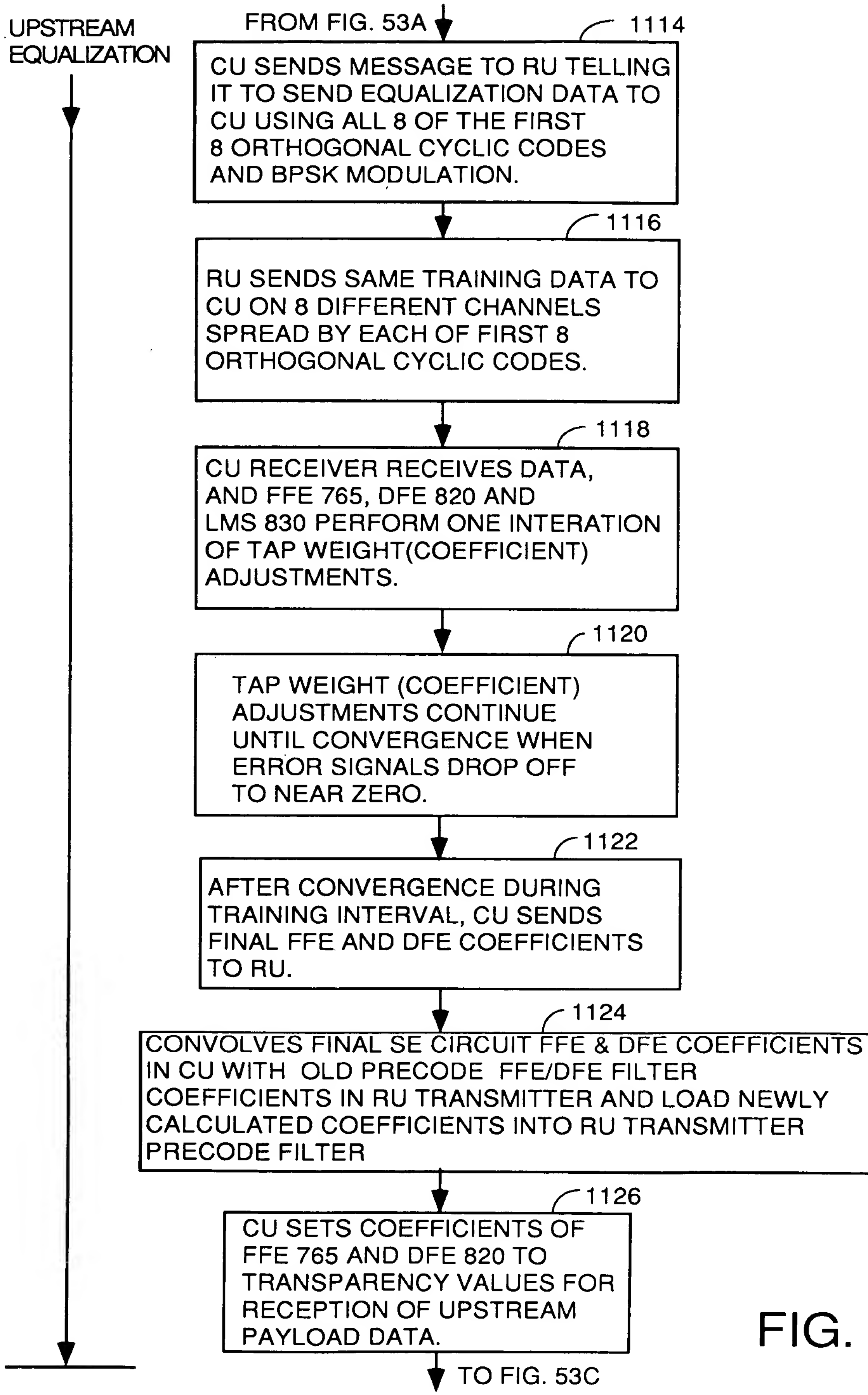

UPSTREAM EQUALIZATION
FROM FIG. 53A
1114
CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.
1116
RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.
1118
CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.
1120
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.
1122
AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.
1124
CONVOLVES FINAL SE CIRCUIT FFE & DFE COEFFICIENTS IN CU WITH OLD PRECODE FFE/DFE FILTER COEFFICIENTS IN RU TRANSMITTER AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU TRANSMITTER PRECODE FILTER
1126
CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO TRANSPARENCY VALUES FOR RECEPTION OF UPSTREAM PAYLOAD DATA.
TO FIG. 53C

FIG. 53B

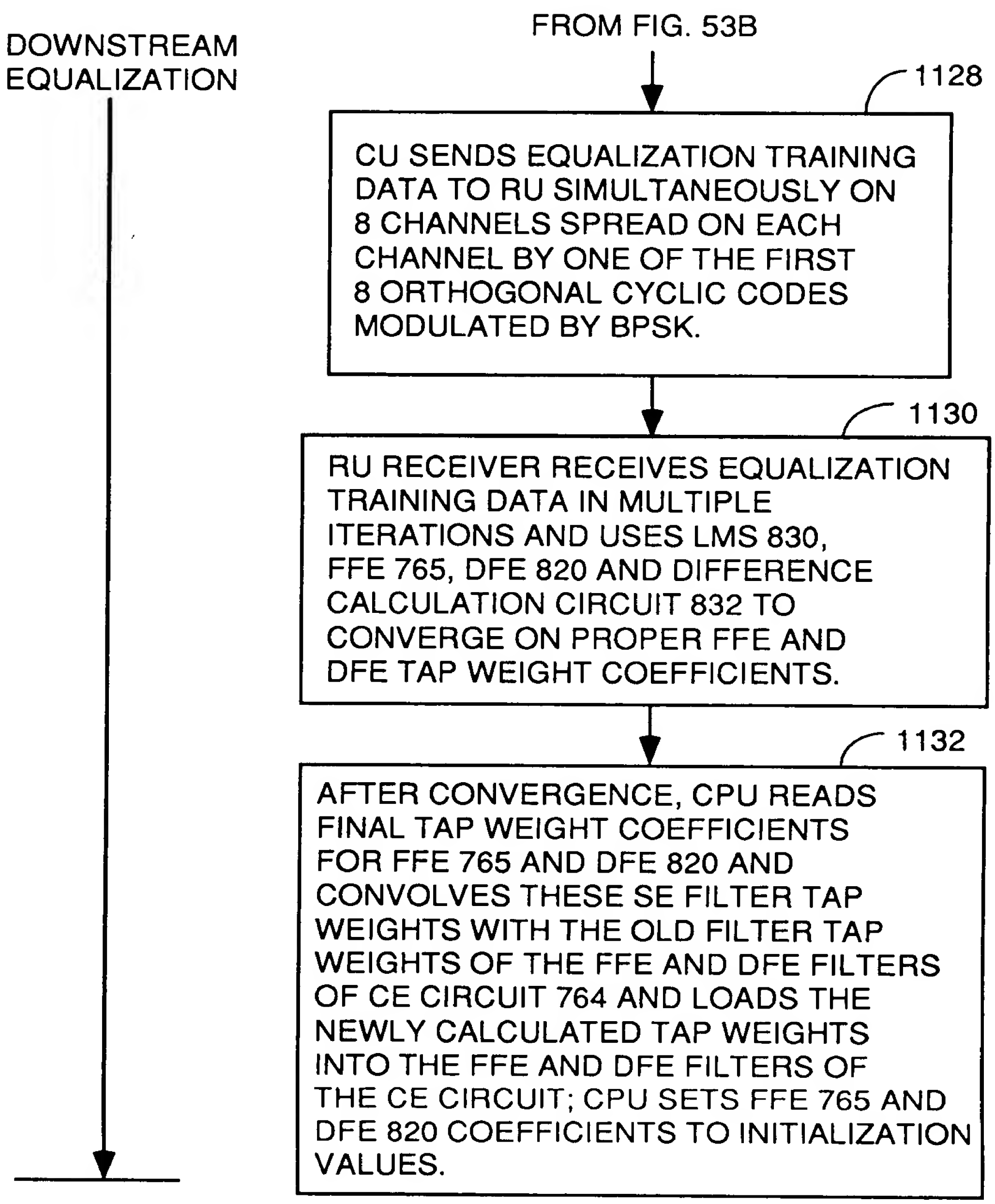
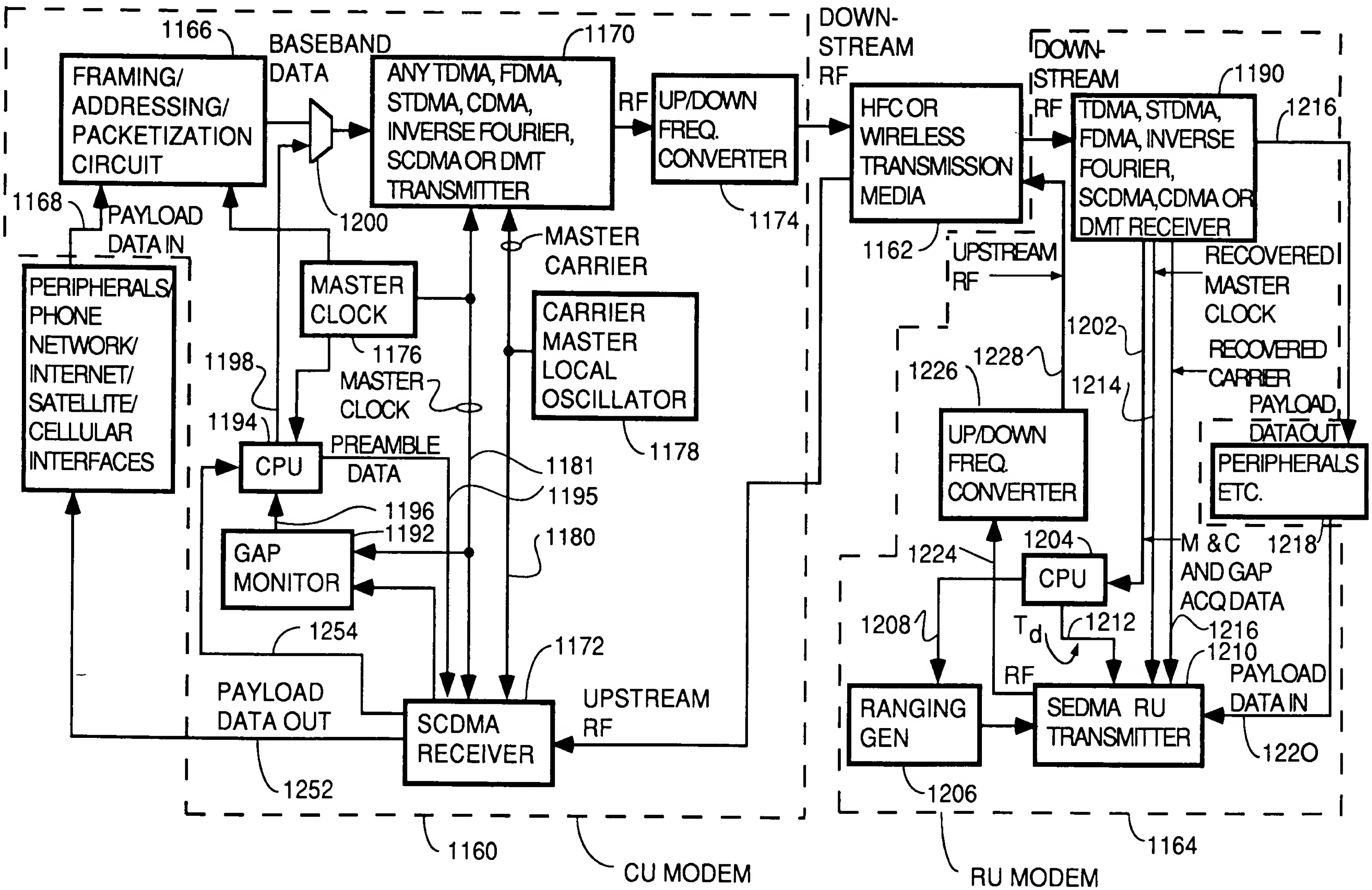
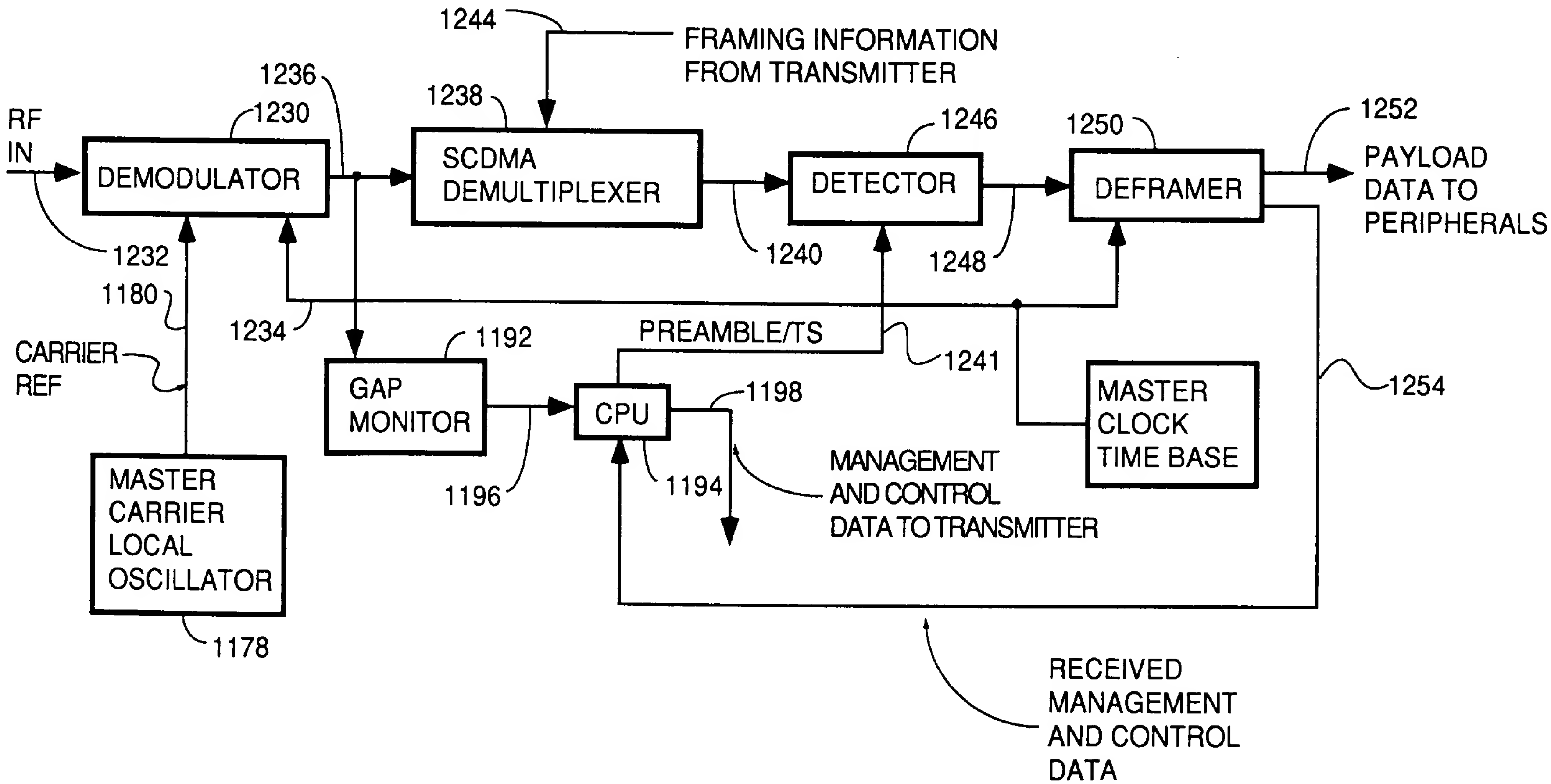

DOWNSTREAM EQUALIZATION
FROM FIG. 53B
1128
CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.
1130
RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.
1132
AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AND DFE FILTERS OF CE CIRCUIT 764 AND LOADS THE NEWLY CALCULATED TAP WEIGHTS INTO THE FFE AND DFE FILTERS OF THE CE CIRCUIT; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 53C



FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
1166
BASEBAND DATA
ANY TDMA, FDMA, STDMA, CDMA, INVERSE FOURIER, SCDMA OR DMT TRANSMITTER
1170
RF
UP/DOWN FREQ. CONVERTER
1174
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
DOWN-STREAM RF
TDMA, STDMA, FDMA, INVERSE FOURIER, SCDMA,CDMA OR DMT RECEIVER
1190
1216
1168
PAYLOAD DATA IN
1200
MASTER CARRIER
PERIPHERALS/ PHONE NETWORK/ INTERNET/ SATELLITE/ CELLULAR INTERFACES
MASTER CLOCK
1176
CARRIER MASTER LOCAL OSCILLATOR
1178
1198
MASTER CLOCK
1194
CPU
PREAMBLE DATA
1181
1195
1196
1192
GAP MONITOR
1180
1254
1172
PAYLOAD DATA OUT
SCDMA RECEIVER
UPSTREAM RF
1252
1160
CU MODEM
UPSTREAM RF
RECOVERED MASTER CLOCK
1202
1226
1228
1214
RECOVERED CARRIER
PAYLOAD DATA OUT
UP/DOWN FREQ. CONVERTER
PERIPHERALS ETC.
1204
1224
CPU
M &C AND GAP ACQ DATA
1218
1208
T_d
1212
1216
1210
RF
PAYLOAD DATA IN
RANGING GEN
SEDMA RU TRANSMITTER
1220
1206
1164
RU MODEM

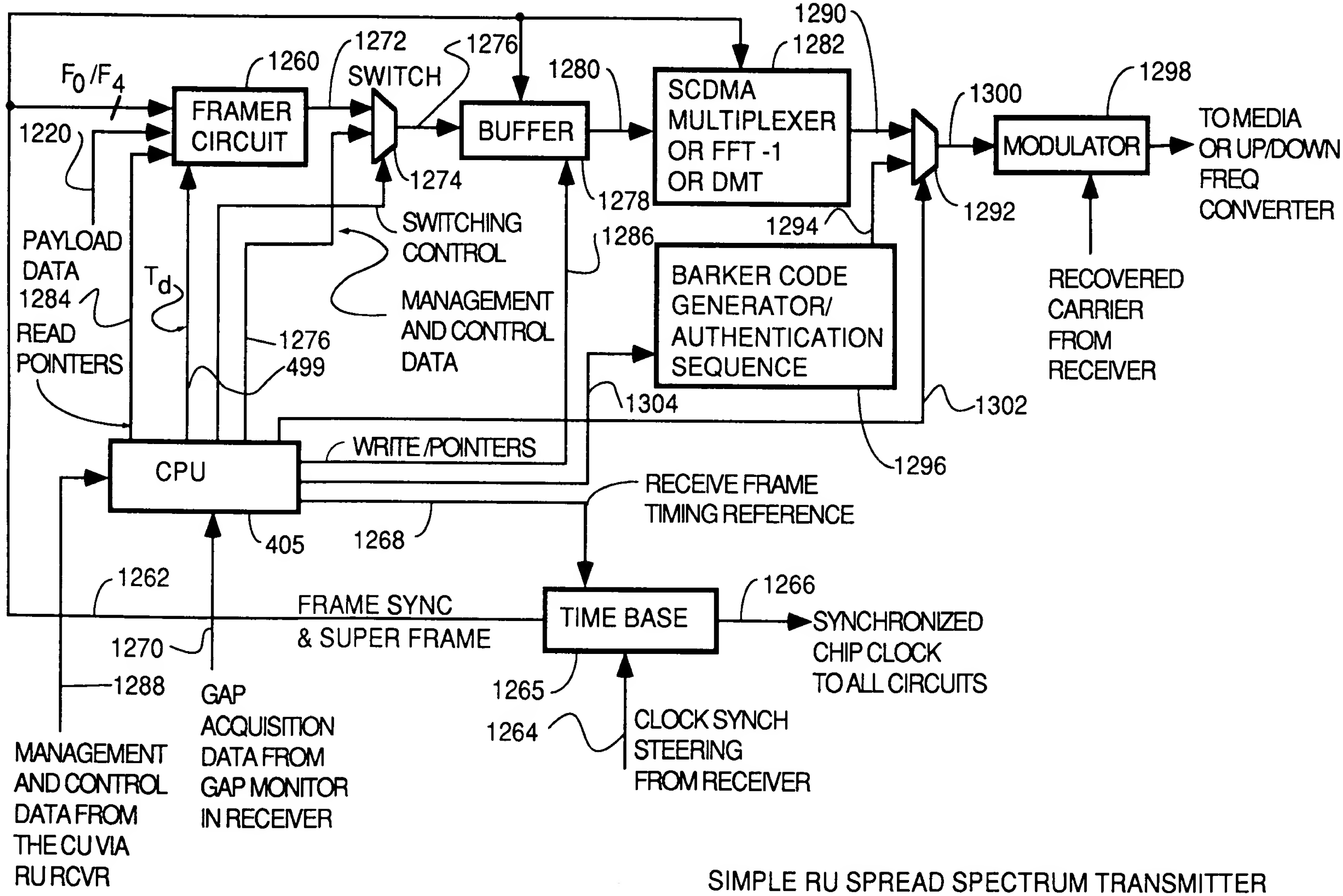
FIG. 54



SIMPLE CU SPREAD SPECTRUM RECEIVER

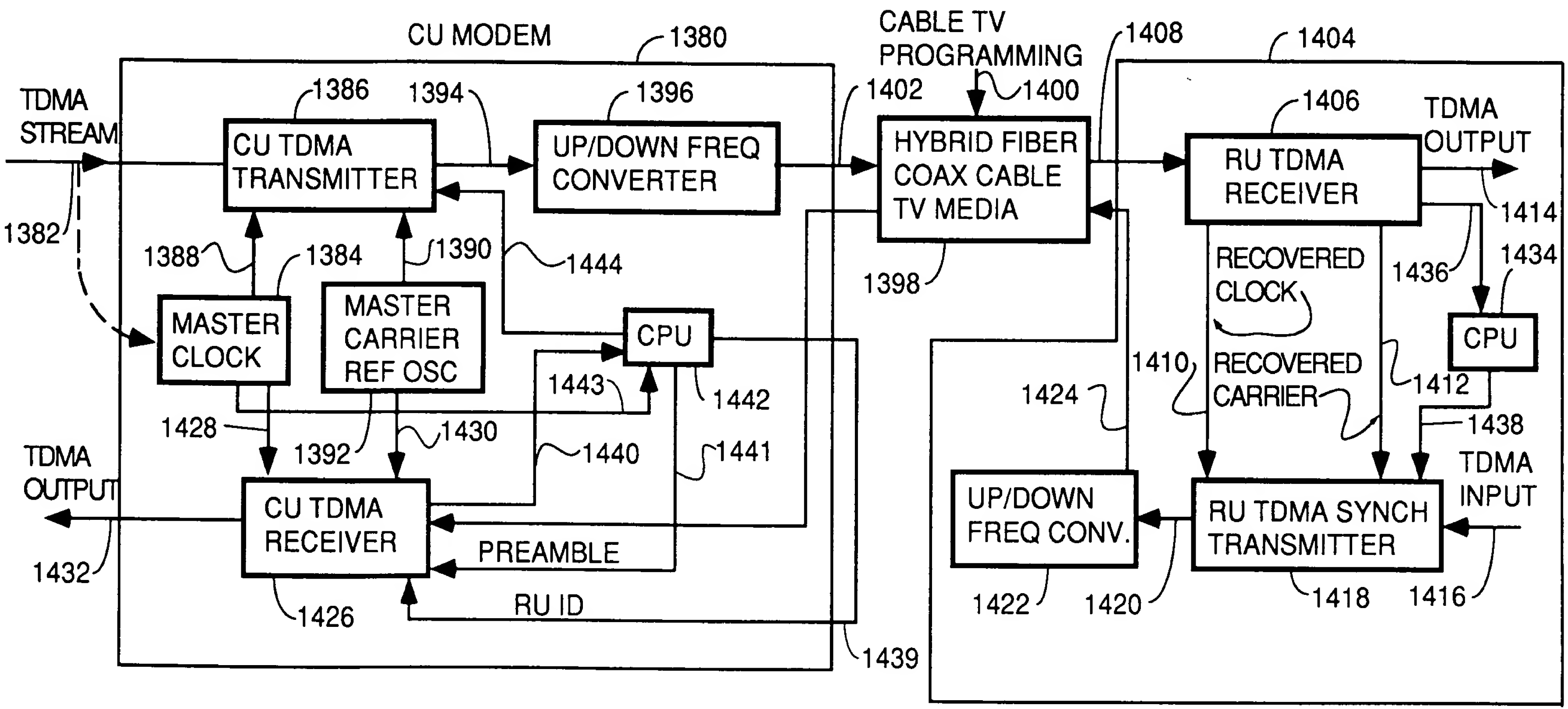
FIG. 55

T02T40"h2265260



SIMPLE RU SPREAD SPECTRUM TRANSMITTER

FIG. 56



SYNCHRONOUS TDMA SYSTEM

FIG. 57

OFFSET	1B ASIC		2A ASIC	
(CHIPS)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

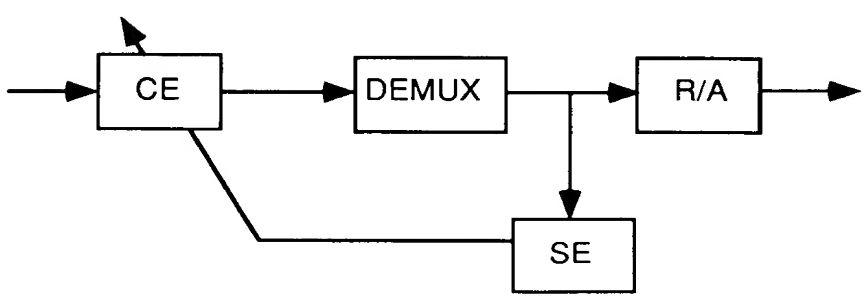
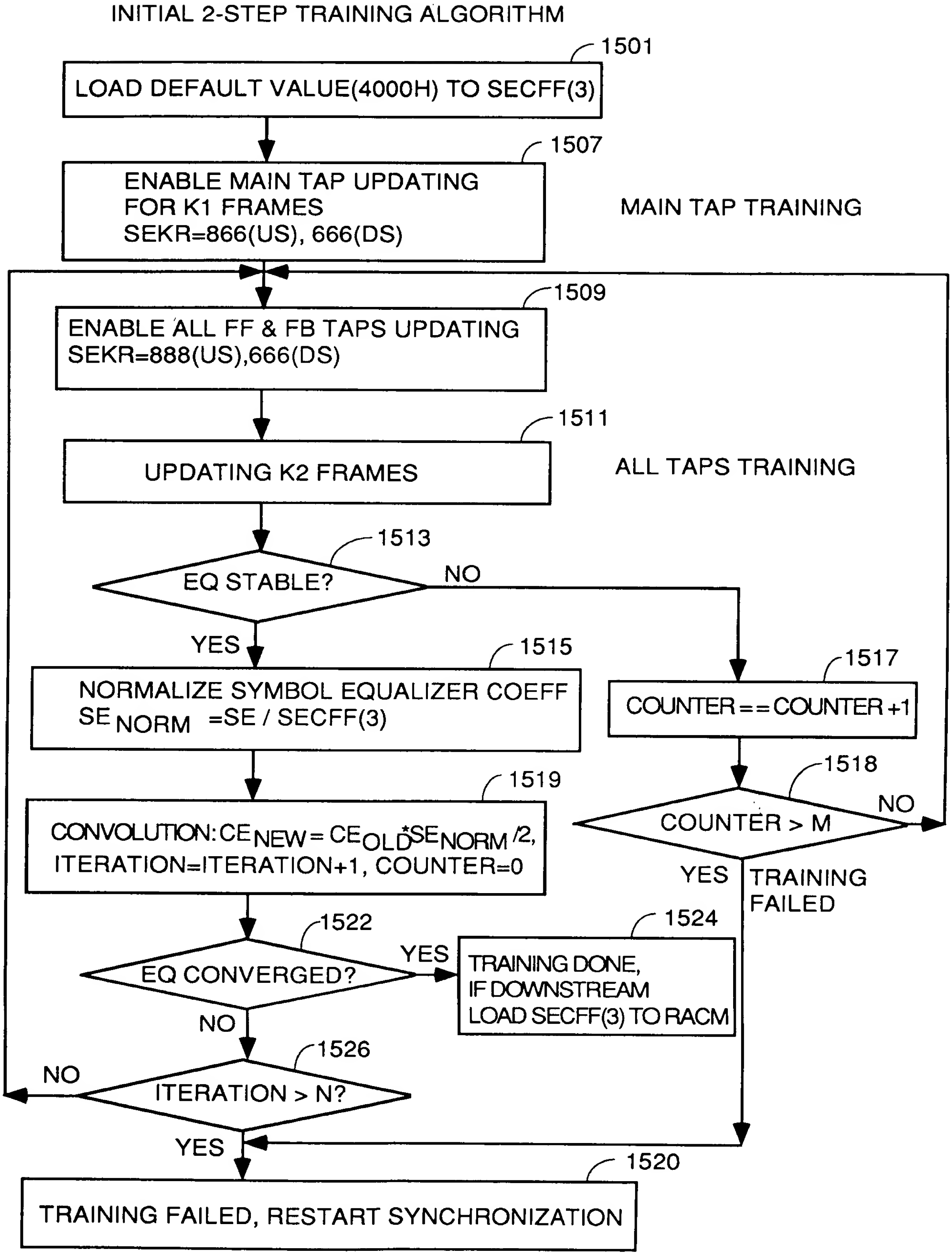


FIG. 59



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

EQ STABILITY CHECK

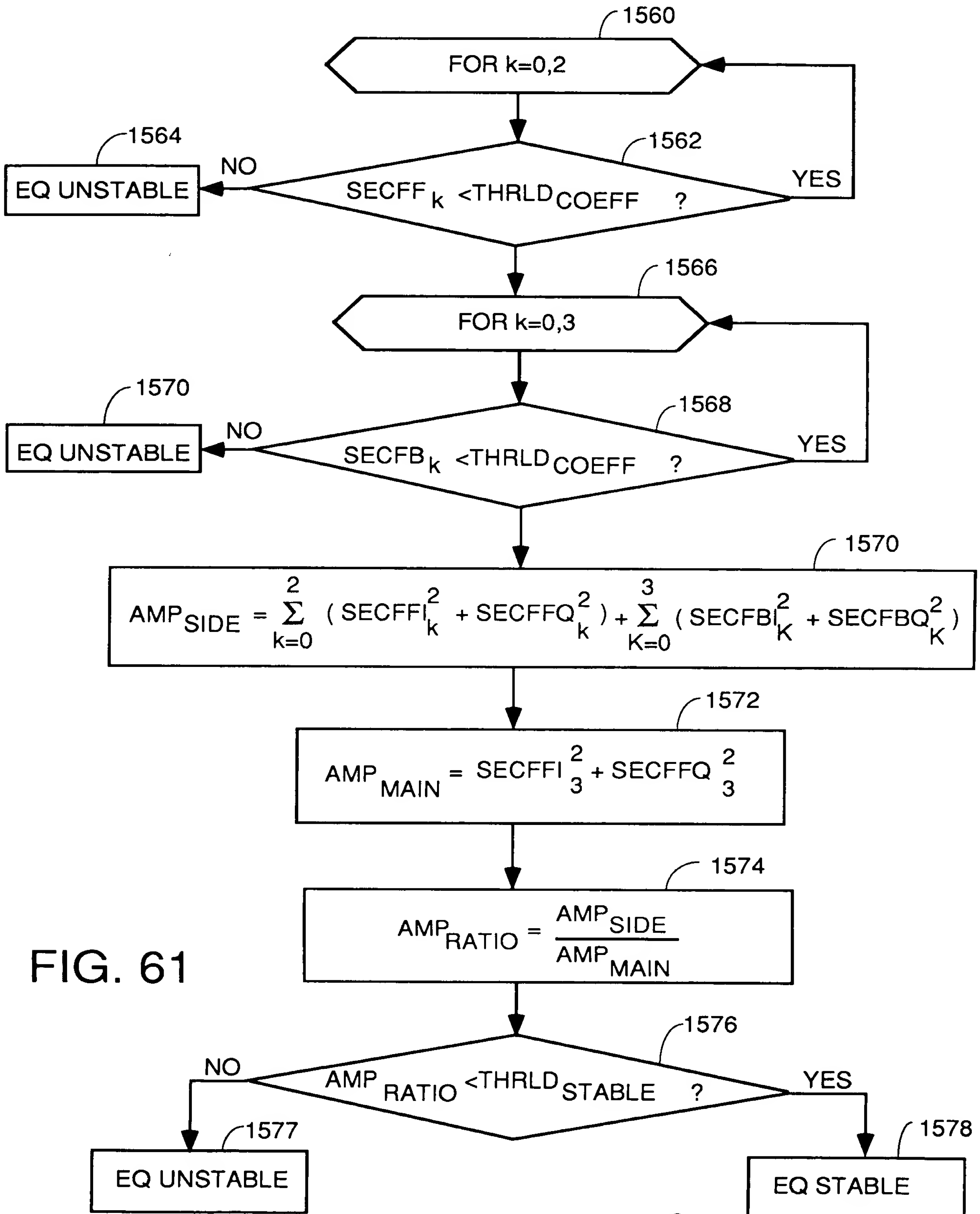


FIG. 61

NOTE: $THRLD_{COEFF} = 7F00H$ $THRLD_{STABLE} = 10^{-3}$

PERIODIC 2-STEP TRAINING ALGORITHM

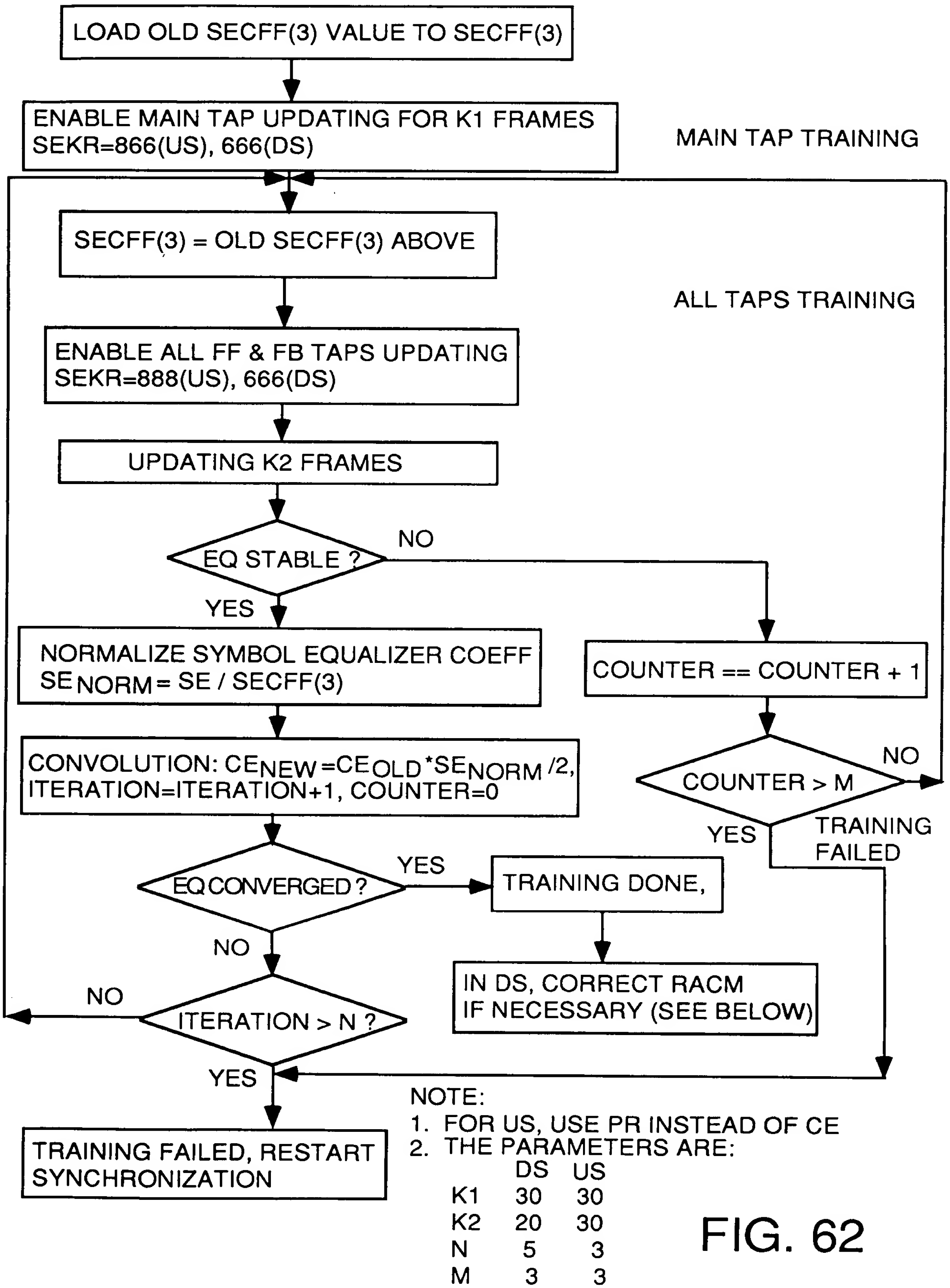
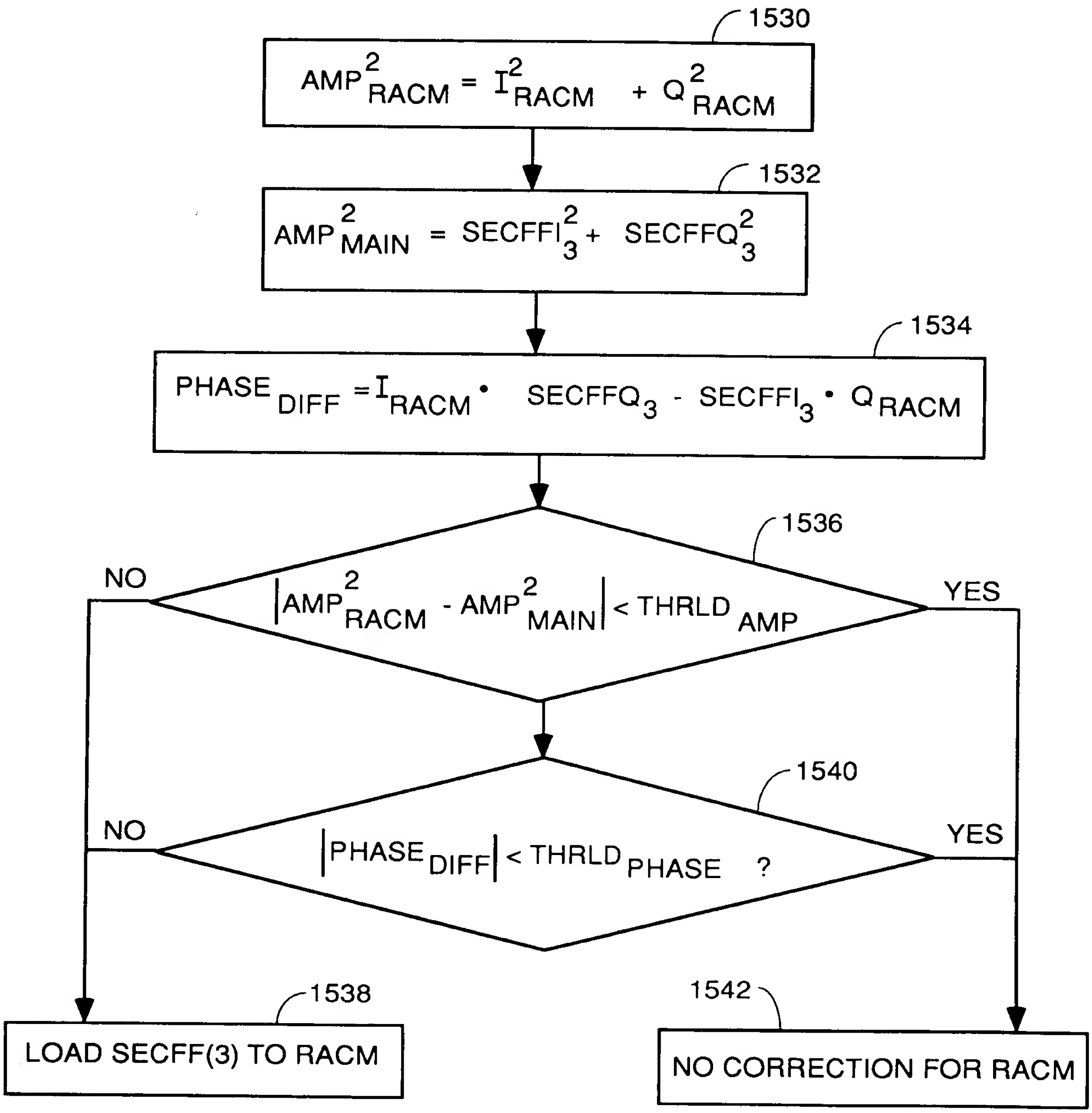


FIG. 62

RACM CORRECTION



NOTE: $THRLD_{AMP}$ = TBD

$THRLD_{PHASE}$ = TBD

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

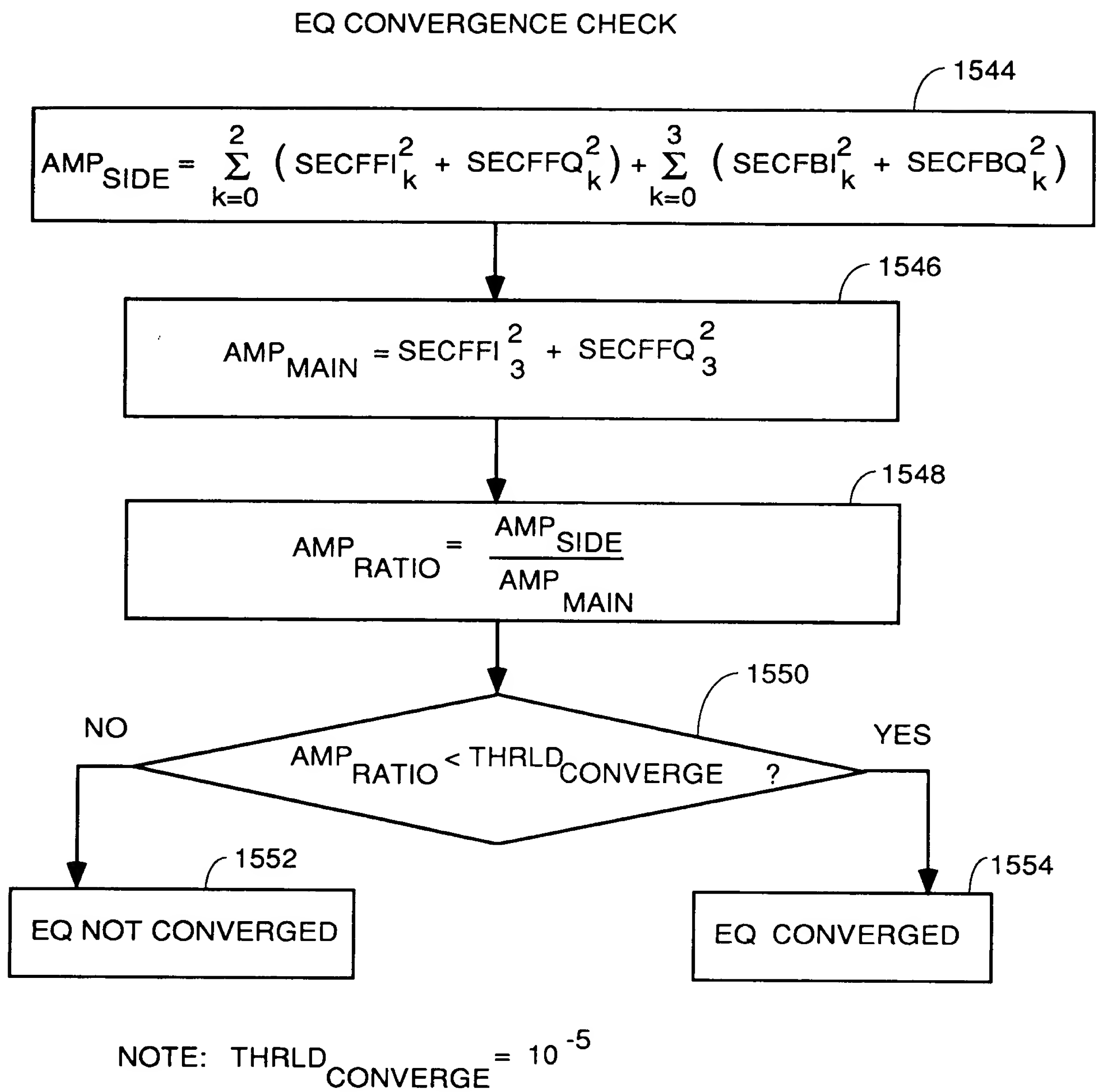
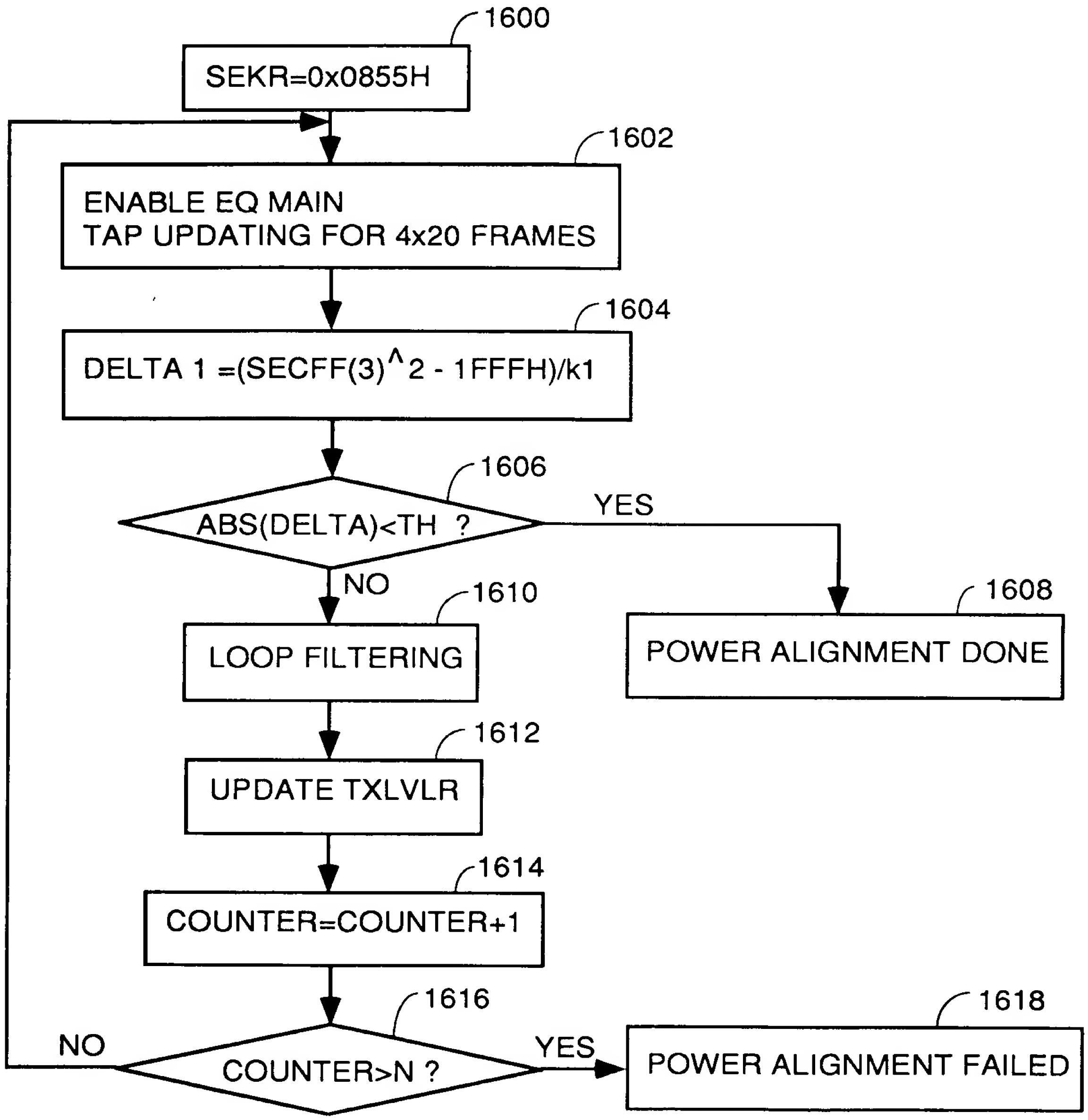

EQ CONVERGENCE CHECK
1544
$AMP_{SIDE} = \sum_{k=0}^{2} (SECFFI_k^2 + SECFFQ_k^2) + \sum_{k=0}^{3} (SECFBI_k^2 + SECFBQ_k^2)$
1546
$AMP_{MAIN} = SECFFI_3^2 + SECFFQ_3^2$
1548
$AMP_{RATIO} = \frac{AMP_{SIDE}}{AMP_{MAIN}}$
1550
$AMP_{RATIO} < THRLD_{CONVERGE}$?
NO
YES
1552
EQ NOT CONVERGED
1554
EQ CONVERGED
NOTE: $THRLD_{CONVERGE} = 10^{-5}$

FIG. 64

POWER ALIGNMENT FLOW CHART



NOTE: TH = 600H
N = 12

FIG. 65

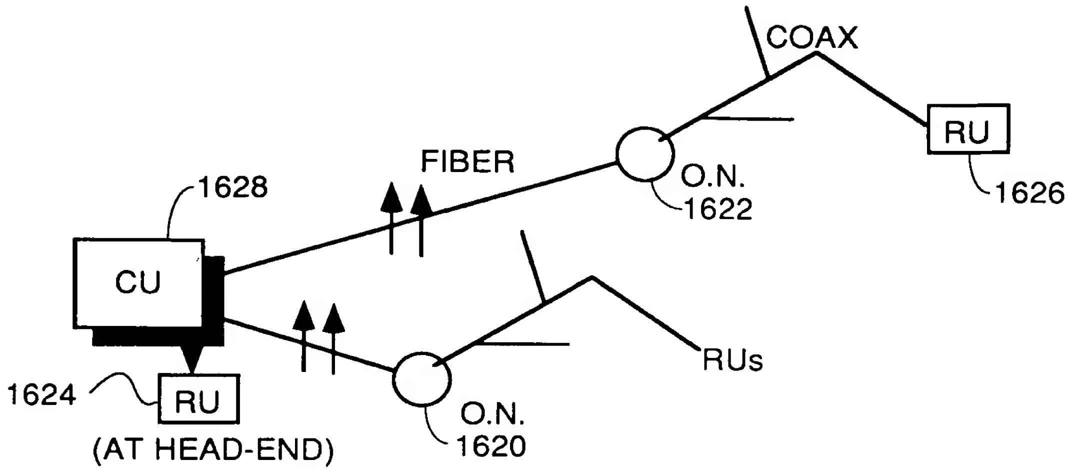
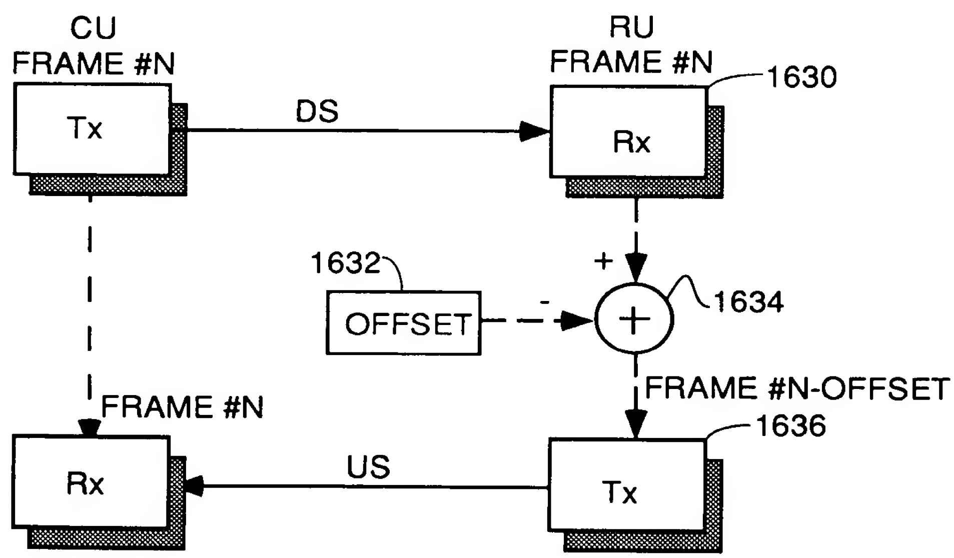


FIG. 66



TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

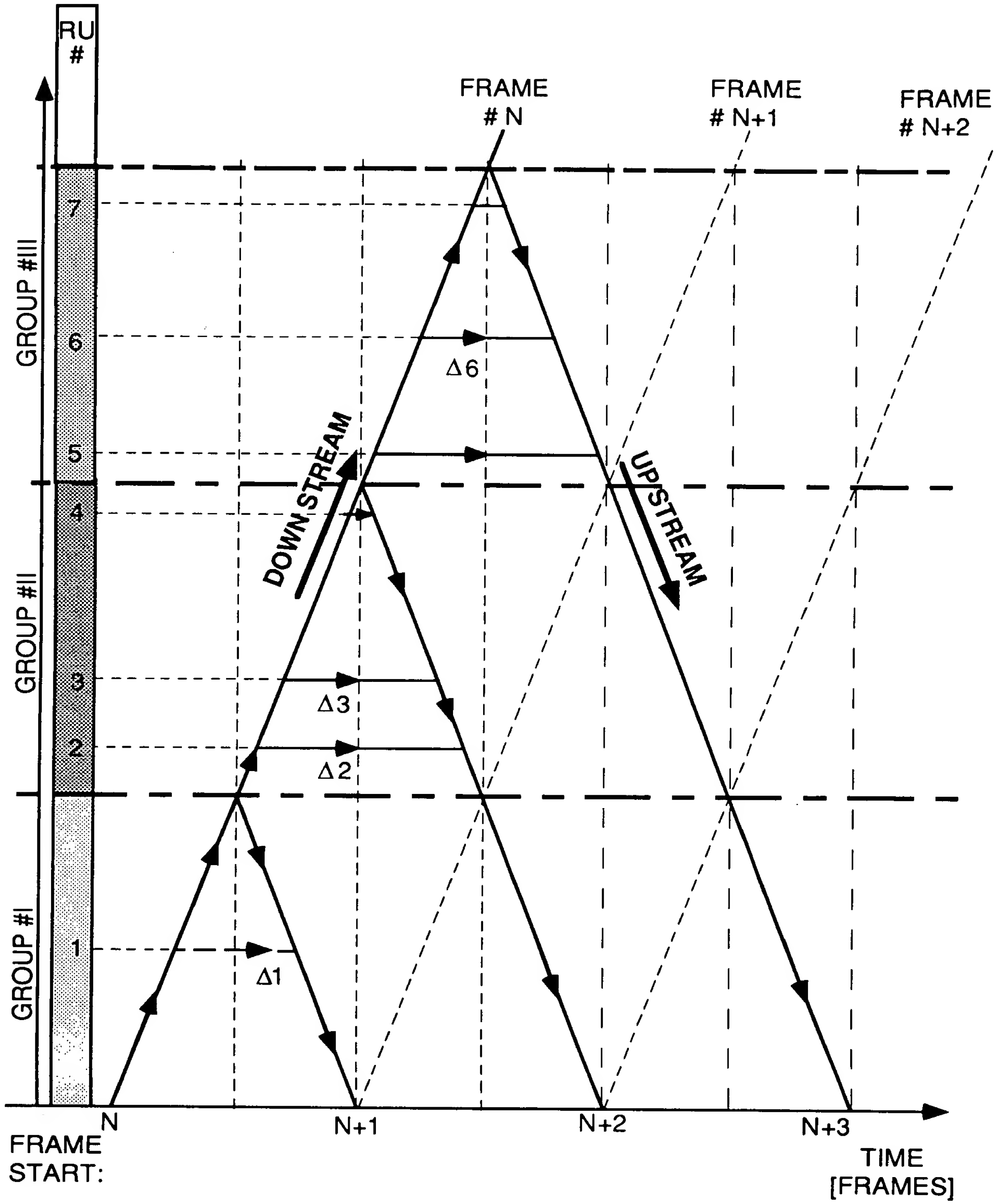
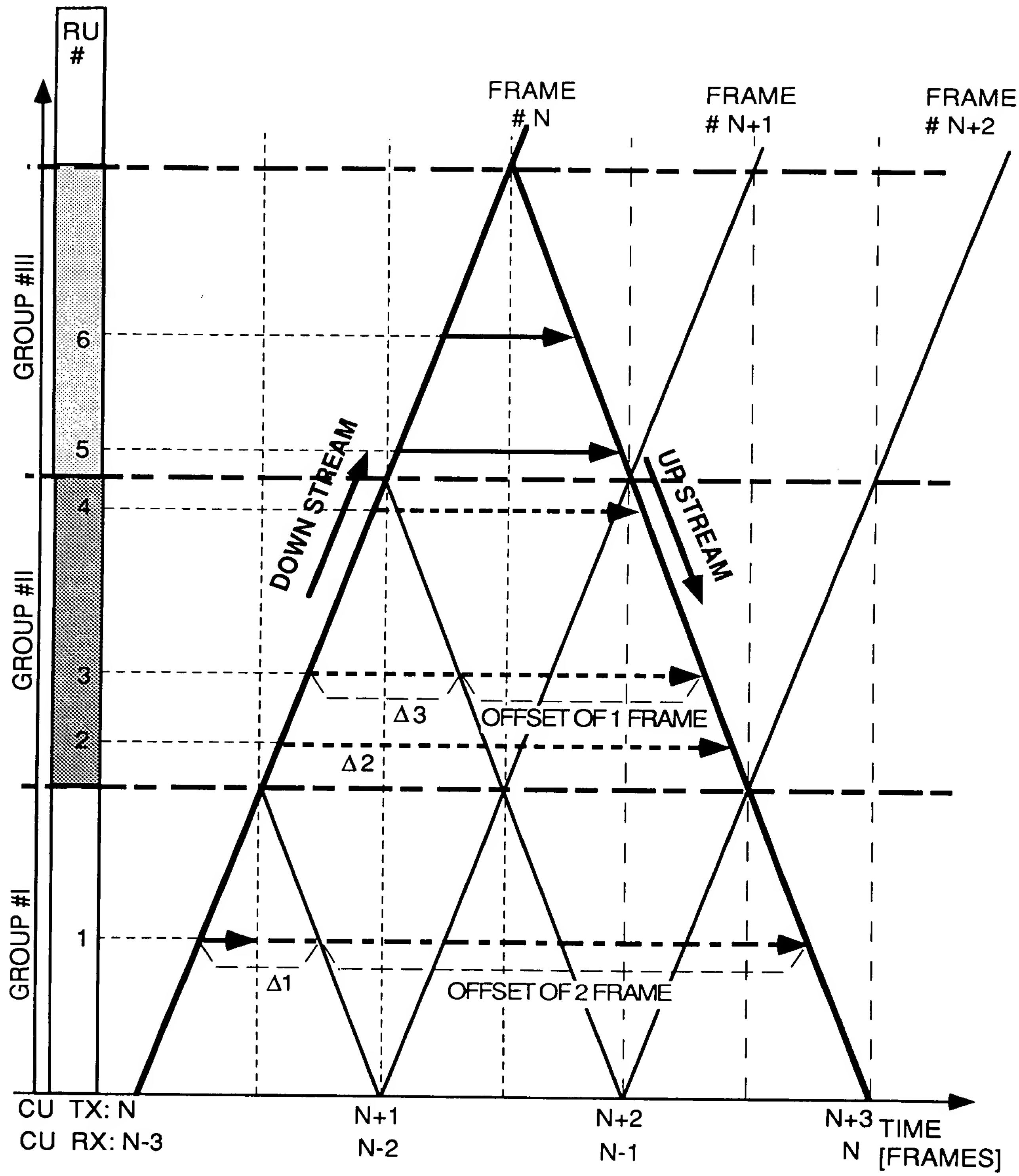

RU #
FRAME # N
FRAME # N+1
FRAME # N+2
7
6
5
4
3
2
1
GROUP #III
GROUP #II
GROUP #I
Δ6
Δ3
Δ2
Δ1
DOWN STREAM
UPSTREAM
N
N+1
N+2
N+3
FRAME START:
TIME [FRAMES]

FIG. 68



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM)
PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

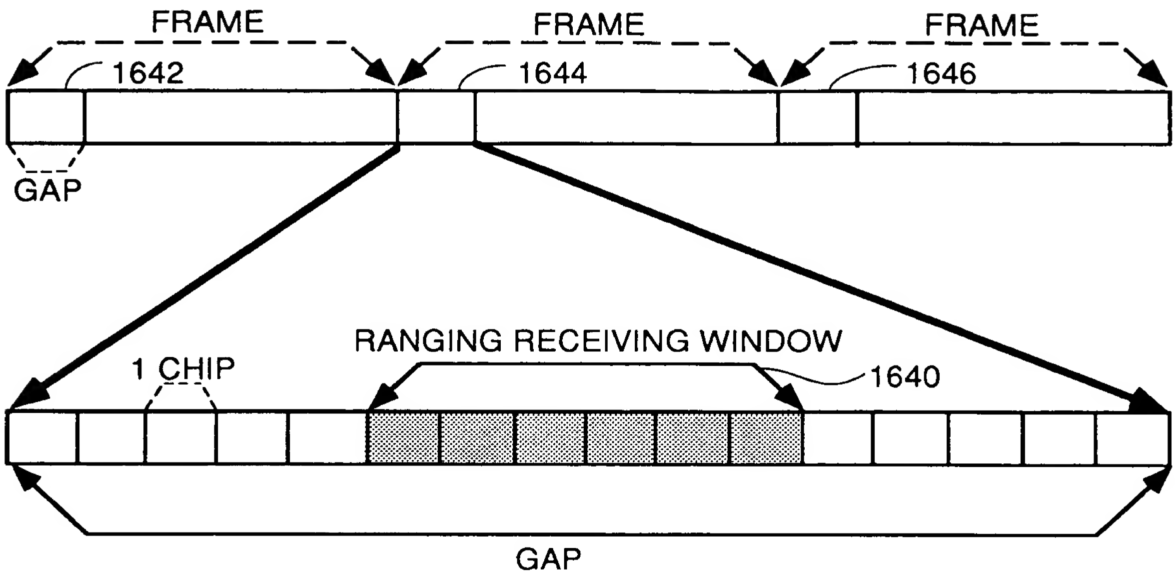
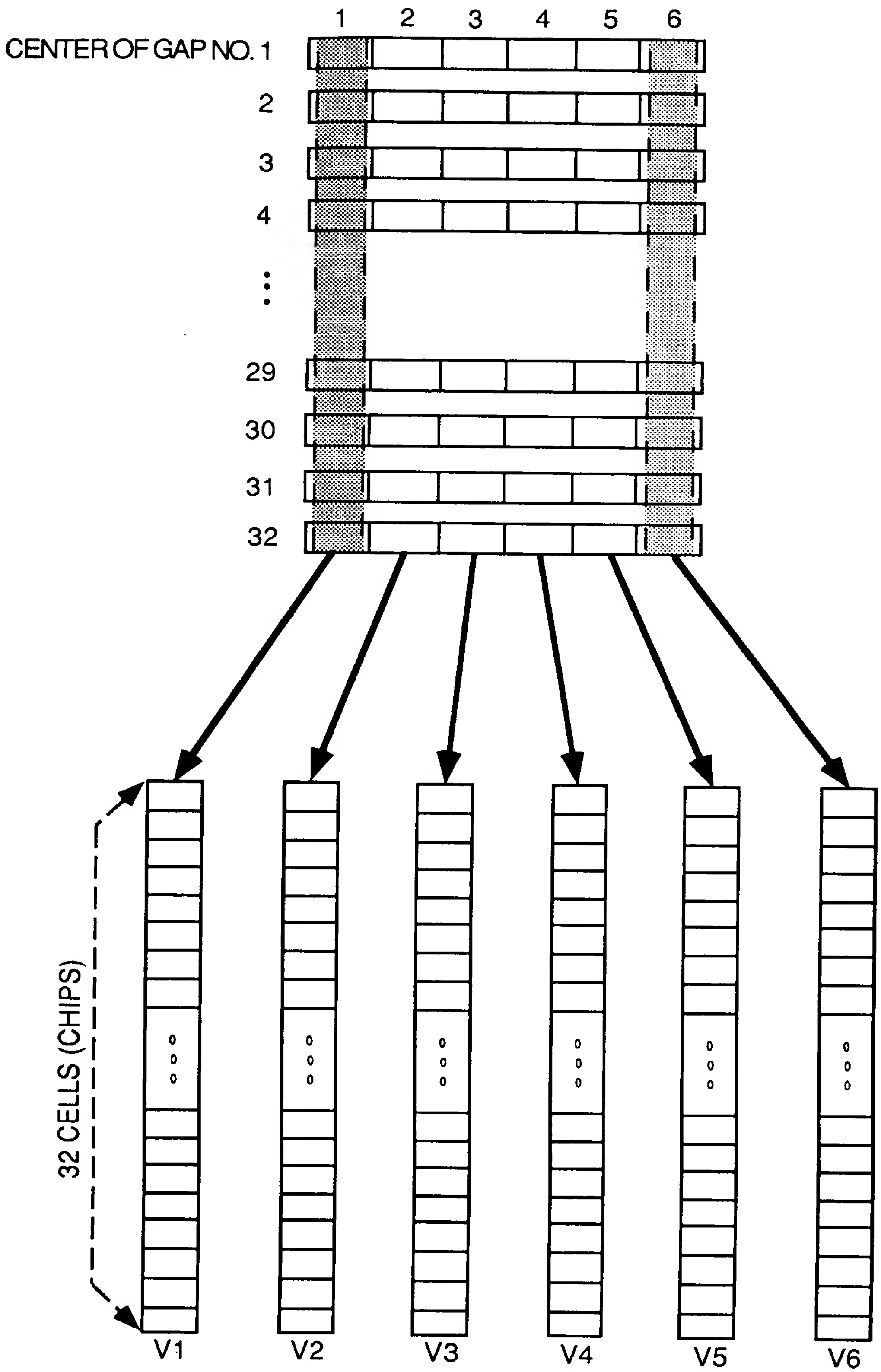

FRAME
FRAME
FRAME
1642
1644
1646
GAP
RANGING RECEIVING WINDOW
1 CHIP
1640
GAP

FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	•••	0
2	1	0	0	1	1	1	1	•••	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	•••	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	•••	

FIG. 72